

An Injection Locked Ring VCO with Enhanced Phase Noise for 2.4GHz Band ZigBee Applications

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Abstract: A low power low phase noise ring voltage controlled oscillator (ring VCO) with subharmonic injection locking is proposed for low power applications in 2.4GHz ISM band, such as ZigBee systems. The injection signal to this VCO comes from a PLL, in which, a replica ring VCO is used. The PLL operates at 1/4th of target frequency and through locking to an available exact reference frequency, provides the control voltage for the second ring VCO. Due to operating at lower frequencies, PLL produces less phase noise, and through injection locking, reduces the phase noise of the second ring VCO that operates at 4× frequency. The target application in this paper, is 2.4GHz band ZigBee, however, it can be used in other applications with similar specifications. The circuit is designed in TSMC 0.18 μm CMOS technology. The phase noise at 3.5 and 10 MHz offsets is -117 and -119 dBc/Hz, respectively, and total circuit consumes 6.1 mW from a 1.8 V supply.

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1. Introduction

Various wireless standards have been developed in the last decade, in reply to the increasing needs of faster and at the same time lower power data transmissions. For those applications, one-chip RF electronics systems are required to reduce production cost. To cater this need, a great effort has been accomplished to develop RF electronics systems using highly scaled advanced complementary metal oxide semiconductor (CMOS) processes.

These processes are advantageous to some circuits and applications such as analog-to-digital (A/D) and digital-to-analog (D/A) converters and digital baseband circuits. However, reduction the scale of RF/analog circuit blocks, such as voltage-controlled oscillators (VCOs), phase-locked loops (PLLs) and power amplifiers is very difficult, because of the presence of inductors that do not scale with advancements in technology [1].

There are two general types of VCOs: Ring VCOs and LC VCOs. Ring-type VCOs (ring VCOs) are more attractive than LC-type VCOs (LC VCOs) because they (ring VCOs) have more scalability and wide-band operation. Besides, they suffer from poor phase noise, which is the most important point in designing a transceiver system. Therefore, ring VCOs cannot be used for some applications, such as wireless LANs and cellular phones. However, if there is a method that can solve the poor phase noise problem, the ring VCOs are the best option for many applications. One of these ways is injection locking technique [2].

Many authors [3-6] have studied the behavior of injection locked oscillators so far. The injection locking technique is also implementable on some other circuits such as clock and data recovery (CDR) circuits, injection locked frequency dividers (ILFD), and injection locked frequency multipliers (ILFM).

This paper presents a frequency synthesizer for ZigBee applications. The proposed frequency synthesizer is composed of a phase locked loop (PLL) and a ring VCO. Since the oscillator with low output frequency have desirable phase noise specification in all offset frequencies [7], we design a low frequency and low phase noise ring VCO in a PLL architecture, so we get a low phase noise signal from the PLL output. Besides, a ring VCO with output frequency of 2.4 GHz is designed such that uses the PLL output frequency for injection locking technique to obtain the same phase noise specification in the PLL output (with little degradation that is negligible). It is obvious that with single stage PLL that has a high frequency and inferior phase noise specification, this aim can't be achieved.

2. Proposed Structure

Figure 1 shows the proposed frequency synthesizer. It is composed of a phase locked loop and a ring VCO out of the loop. The PLL works with a reference frequency of 1.25 MHz and a divider with division ratio of 481-496. So, output signal of the PLL has a frequency range from 601.25 MHz to 620 MHz. Channel selection is done by this PLL. It uses a ring VCO that has low phase noise specification. In

reality, we use this fact that in low frequencies obtaining a low phase noise characteristics is easier than high frequency oscillator. This output signal is used to inject to a ring oscillator that is out of loop and has the central frequency of 2.4 GHz. Besides, it uses the control voltage of the loop VCO to adjust its frequency.

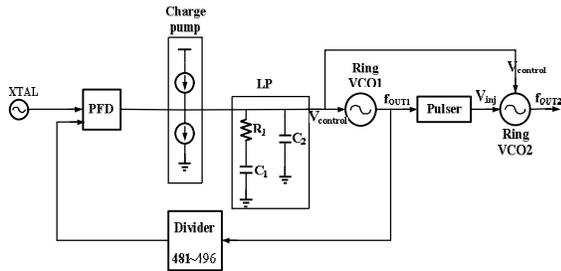


Figure 1. Proposed structure

On the other words, $V_{control}$ of 1V generates the frequency of 610 MHz for the internal VCO, and produces 4×610 MHz for external VCO (in this way all of the ZigBee channels is covered). It is necessary to mention that a small offset is tolerable, because the output signal of the PLL pulls the output of the VCO to the desired frequency. As a result, we have the phase noise specification of the PLL in the external VCO output with negligible degradation.

3. Phase Noise Reduction with Subharmonic Injection Locking

Figure 2 shows a conceptual oscillator that its tank resonates at frequency of $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$, thus contributing no phase shift. The inverter buffer is ideal and within the transistor provides 360° phase shift around the feedback loop. If an additional ϕ_0 phase shift inserted in the loop, the oscillation frequency can't remain in ω_0 because the total phase shift deviates from 360° .

Phase shift of ϕ_0 can be occurred by injecting a sinusoidal current of I_{inj} with proper amplitude and frequency. In this condition the oscillation frequency is not ω_0 and the oscillator works at new frequency of ω_{inj} . The oscillator in this condition is called injection locked oscillator [4].

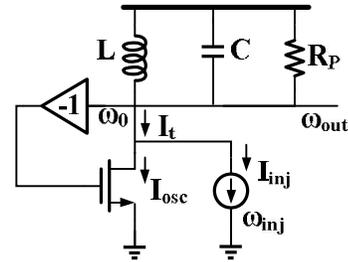


Figure 2. Conceptual oscillator with injection locking [4].

The range of ω_{inj} in which injection locking holds is called locking range, ω_L , and expressed by the following equation

$$\omega_L \approx \frac{\omega_0 I_{inj}}{2Q I_{osc}} \tag{1}$$

Where Q denotes the quality factor of the tank. In fact the overall lock rang is in $\pm \omega_L$ around the ω_0 [4].

In subharmonically injection-locked oscillators, the frequency of injection signal is $1/N$ of the output frequency of the oscillator. The lock range is determined by the power of the N^{th} superharmonic of the reference signal as

$$\omega_L = \frac{\omega_{out}}{2Q} \cdot \sqrt{\frac{P_{injN}}{P_0}} \tag{2}$$

where Q is the quality factor of the oscillator, ω_{out} represents the output frequency of the oscillator under the injection locked condition, P_{injN} is the N^{th} harmonic power of the reference signal, and P_0 is the free-running output power of the oscillator [2].

In this condition, Equation 1 becomes to

$$\omega_L \approx \frac{\omega_0 I_{inj}}{2Q I_{osc} N} \tag{3}$$

In general, I_{inj} is the injected current to the delay cell and I_{osc} is required tail current of the VCO for oscillation [5].

Locking range and phase noise of injection signal determine the phase noise characteristics of the injection-locked oscillator. If locking range is large enough, the phase noise specification of the injection locked oscillator output follows the phase noise specification of the injection signal (related to the N factor, the output phase noise is larger than injection signal phase noise) [4],[8]. Figure 3 shows how phase noise reduces with injection locking .

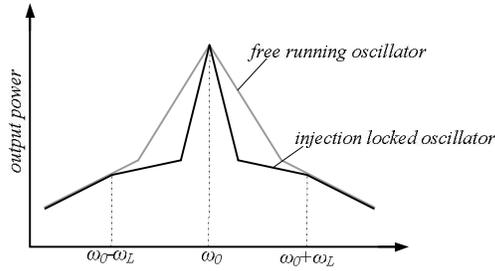


Figure 3. Phase noise reduction with injection locking [5].

Ring VCOs have lock range of injection locking wider than that of LC VCOs because they have low quality factor (Equation 2). As a result, injection locking technique is an effective way to improve phase noise characteristic of ring VCOs.

Figure 4 demonstrates the reason why in injection-locked oscillators the jitter, namely phase noise characteristics, can be reduced. The jitter will be spread over time when a VCO is in the free-running situation due to thermal noise and flicker noise. When a free running oscillator is locked onto a low phase noise signal every $1/f_{inj}$ the edge of the output signal of the oscillator is forced to be aligned to the injection pulse edge, as a result the jitter no longer accumulates [5].

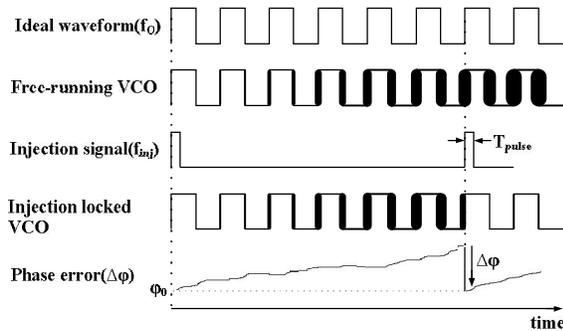


Figure 4. Changes in phase error $\Delta\phi$ when phase corrections are made using injection signals [5].

4. Injection Signal Specification

There are several ways to injecting a signal to the VCO. One of them is use of an NMOS switch that applied between differential nodes of the VCO. When injection pulse becomes high, the switch turns on and differential nodes shorts, consequently phase noise reduction occurs [9].

Since this way uses the shorting between the differential nodes, duration of correcting pulse has limitation. In reality, oscillation period makes this limitation so that pulse with width smaller than rise/fall time of the output signal of the VCO is

suitable for injecting. In otherwise, if injection pulse width is too small, a small current flows through the switch and injection locking doesn't have enough energy for correcting the phase, even locking process may be failed. On the other hand, if the width of the injection pulse is larger than the rise/fall time of the output signal of the PLL, a large amount of current will be injected to the differential nodes and a large rotation in phase signal or a large spurious level may be occurred [2].

Moreover, the oscillation may be prevented due to adding in-phase energy to the oscillators by injection and weakens the negative conductance circuits [2],[4].

In the proposed frequency synthesizer, since correction signal is injected to the external VCO and its output frequency is 2.4 GHz, the injection pulse width is 50 ps. This signal is produced by the circuit is shown in Figure 5. Output frequency of this circuit is double of its input frequency that makes injection locking process more effective.

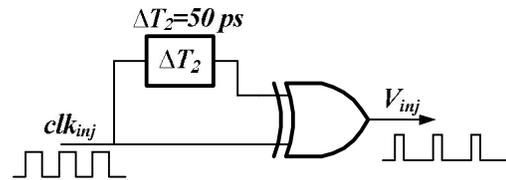


Figure 5. Pulse generator circuit

5. Building Blocks of Frequency Synthesizer

5.1. VCO

Figure 6 shows the block diagram of the Ring VCO is used in PLL1 (VCO1) and VCO2. Figure 7 shows delay cell schematic of each of them. The performance and the function of this type of ring VCO is explained in [10] completely.

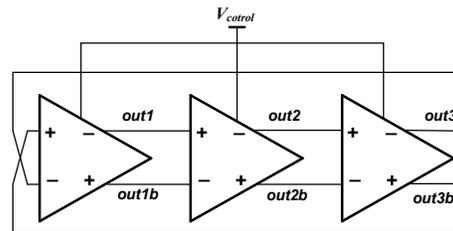


Figure 6. The block diagram of the Ring VCO is used in PLL1 (VCO1) and VCO2.

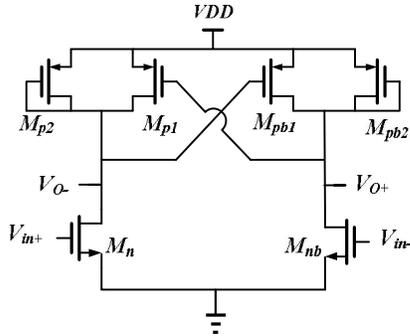


Figure 7. The delay cell schematic of ring oscillators.

The delay cell includes an NMOS transconductance pair, a PMOS cross-coupled load, a PMOS diode pair for the best power-consumption efficiency [10].

Based on the three stage topology for the VCO2 the oscillator loop gain can be expressed as

$$H(s) = -\left(\frac{g_{mn1}}{(G_{ds} + g_{mp2} - g_{mp1}) + sC_L}\right)^3 \quad (4)$$

where $G_{ds} = g_{dsn1} + g_{dsp1} + g_{dsp2}$ is the resistive load because of the channel-length modulation. The negative operator is due to exchanging polarity of the three stages. Based on the Barkhausen criteria, each delay cell provides 60° phase shift and a unit gain at the oscillation frequency. The consequence phase condition requires $G_{ds} + g_{mp2} - g_{mp1}$ be much smaller than sC_L [10].

But this structure has a very high VCO gain (K_{VCO}). As K_{VCO} increases, PLL performance characteristics, such as the stability of the loop, and spurious levels in VCO output signal are degraded. Large loop filters are needed to resolve these problems. On the other hands, if the K_{VCO} is very large for VCO2, adjusting its output frequency according to internal VCO frequency will be very difficult or impossible. The circuit shown in Figure 8 is used to decrease the VCO gain and increase the linearity of K_{VCO} . By adjusting R_1 and R_2 the desired K_{VCO} is provided. In addition, this circuit is used to provide the supply voltage (V_{ctrl}) for the VCO.

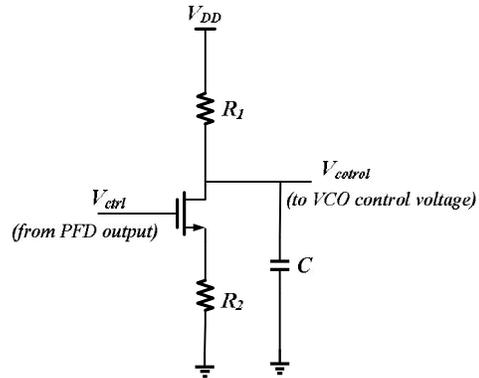


Figure 8. The circuit is used to decrease the VCO gain and increase the linearity of K_{VCO} .

VCO1 has the same general function of VCO2 except that uses the a very small capacitor to decrease the oscillation frequency and improve the phase noise characteristic .

5.2. PFD and Charge Pump

Both of the two stage PLLs, PLL1 and PLL2 use the PFD proposed in [12]. This is a novel PFD that prevents generating the reset signal when the input phase error is out of the range of $[-\pi, \pi]$. As a result, this PFD eliminates the “blind zone” completely and so reduces the settling time of the loop [12]. The nonlinear transfer characteristics of this PFD is shown in Figure 9.

Two stages of PLLs use a simple charge pump that is introduced in [7]. The circuit of this charge pump is shown in Figure 10.

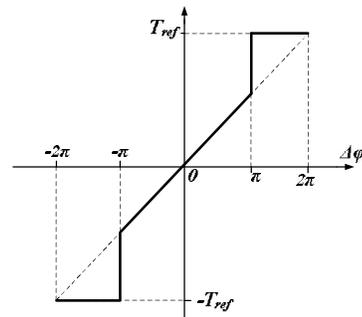


Figure 9. The nonlinear transfer characteristics of the PFD [12].

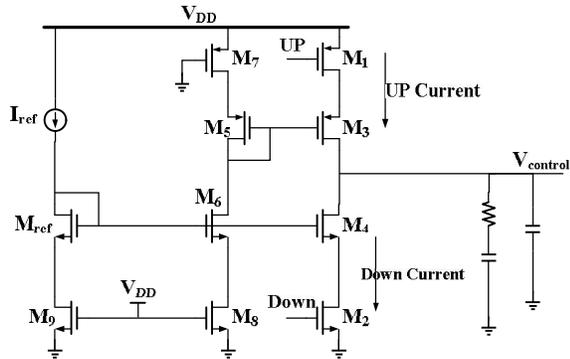


Figure 10. charge pump circuit [7].

5.3. Frequency Divider

PLL1 uses a new low power frequency divider proposed in [13]. It divides the input frequency to 481-496 and so covers all of the ZigBee channels.

6. PLL Design

All of the building blocks of the frequency synthesizer explained in last parts. This section pays to low pass filter designing. The second order filter is used for the PLL (the schematic of this filter is shown in Figure 1). The values of the resistor and capacitors for the PLL is:

$$R=353 \text{ k}\Omega, C_1=20 \text{ pF}, C_2=4 \text{ pF}.$$

7. Simulation Results

This frequency synthesizer is designed in 0.18 μm TSMC technology and simulated by ADS. Simulation results are for channel 12 with frequency of 2.46 GHz. In this condition PLL1 output frequency is 615 MHz.

Figure 11 shows the spectrum of PLL1 output frequency. The spur rejection at 5 and 10 MHz is -54 and -62.4 dB, respectively that satisfies ZigBee specification remarkably. Of course, it is spur rejection for the PLL output signal, but as the VCO out of the PLL (VCO2) has an injection signal with center frequency of 1.2 GHz, its spurs are occurred at harmonics of 1.2 GHz and the spurs of the PLL output spectrum emerge around these harmonics. It is necessary to mention that the spurs around first harmonic are important and higher order harmonics and spurs around of them are eliminated by transceiver filters.

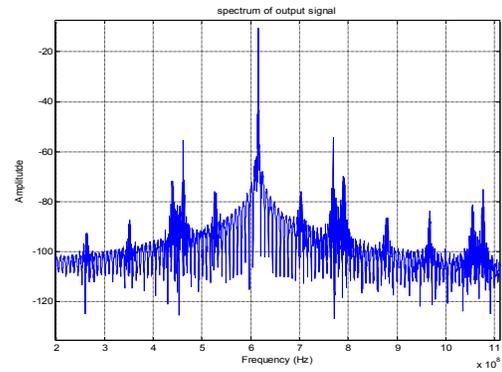


Figure 11. The spectrum of PLL1 output frequency

Figure 12 shows the phase noise of the free running VCO and PLL. As depicted in this figure, after frequency about 1 MHz the phase noise characteristic of VCO and PLL overlap together. PLL output phase noise at 1 MHz offset frequency is -106.8 dBc/Hz.

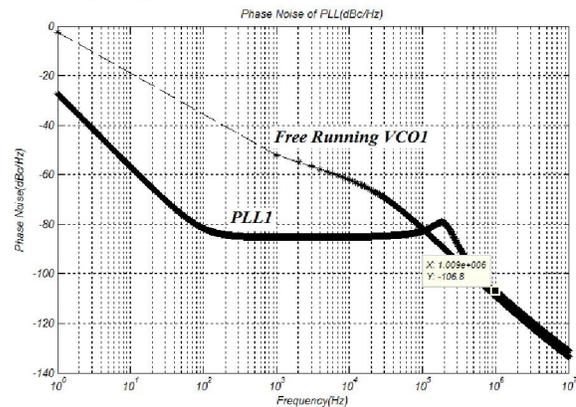


Figure 12. The phase noise of free running VCO1 and PLL1.

For simplicity a single clock source with equivalent jitter to the output phase noise of the PLL (rms jitter=3.6 picoseconds by integrating on 10 Hz to 100 MHz offset phase noise) is used instead of PLL output in simulating VCO2. Figure 13 shows phase noise characteristics of VCO2 with and without injection. The phase noise at 3.5 and 10 MHz offset frequencies is -117 and -119 dBc/Hz respectively.

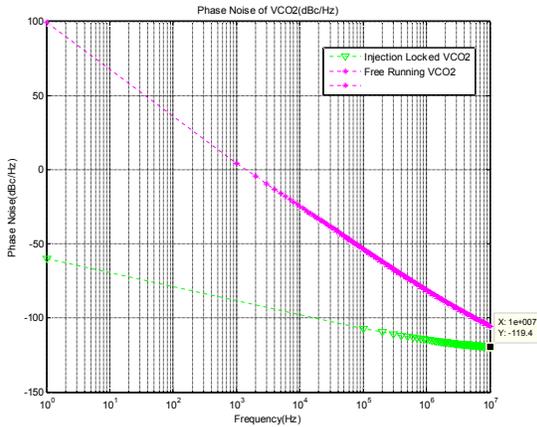


Figure 13. Phase noise characteristics of VCO2 with and without injection.

PLL1 has 25 μ s settling time and locking time for the VCO2 is about 20 ns, so total frequency synthesizer has 25 μ s settling time.

PLL1 uses 2 mA and VCO2 uses 1.4 mA, consequently total frequency synthesizer has 6.1 mW power consumption.

As frequency synthesizer subsystems such as PFD, charge pump, LPF, frequency divider are not sensitive to temperature and process (in this application) and VCO is the most sensitive subsystem, for testing synthesizer in technology corners, just VCO is simulated. Figure 14 shows VCO1 behavior in the technology corners.

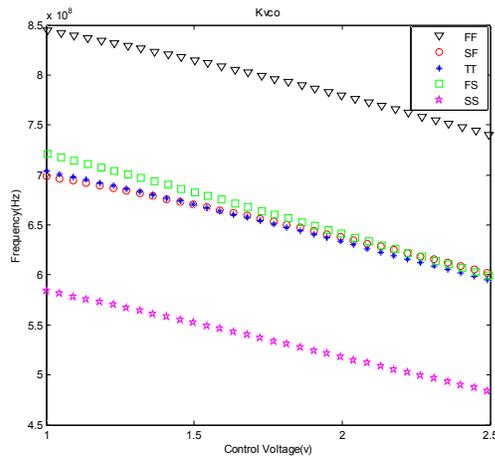


Figure 14. VCO1 behavior in the technology corners.

As depicted in this figure, the value of K_{VCO} has a little change in 4 corners, but the frequency has about 20% change in the corners of fast-fast and slow-slow. These variations are not very important because by varying the supply voltage the frequency can be set to the desirable value.

Figure 15 shows VCO2 behavior in the corners of technology. As mentioned before about VCO1, in this case the K_{VCO2} is almost without change in the technology corners and just the values of the frequency at fast-fast and slow-slow corners varies around 20%. This variation is compensable by a little change in the supply voltage value. On the hand, in this frequency synthesizer the ratio of K_{VCOs} ($\frac{K_{VCO2}}{K_{VCO1}} = 4$) is important that is almost fixed.

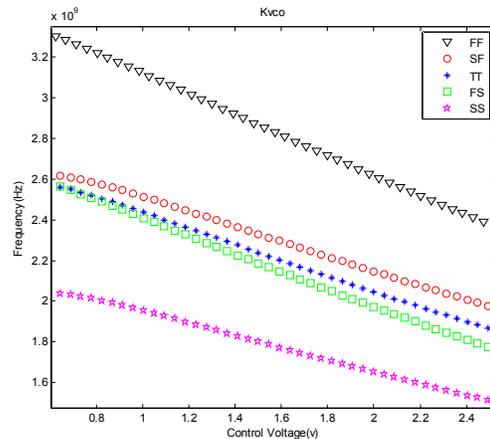


Figure 15. VCO2 behavior in the corners of technology.

Table 1 demonstrates a performance summary and a comparison of proposed frequency synthesizer with other zigbee synthesizers.

Table 1: Performance summary and comparison of proposed frequency synthesizer with other zigbee synthesizers

	This work	[14]	[15]	[16]
Frequency (GHz)	2.4-2.48	2.4-2.48	5	2.4-2.48
Technology (μ m)	0.18	0.18	0.18	0.18
Supply voltage (volts)	1.8	1.2	1.8	1.8
VCO type	Ring	LC	LC	LC
Settling time (μ s)	25	500	-	25
Phase noise (dBc/Hz)	-117.6@ 3.5MHz -119.4@ 10MHz	-112 @1MHz	-135 @3MHz	-108.55 @1MHz
Spur rejection (dB)	-54@ 5MHz -62.4@ 10MHz	-60 @5MHz	-64 @2MHz	-40.84 @5MHz
Power consumption (mW)	6.1	3.5	19.8	7.95

This frequency synthesizer has performance comparable to other synthesizers, but its most important specification is the use of ring oscillator that has small dimensions, is low cost and it can scale with the technology and has low tolerance in fabrication.

8. Conclusions

In this paper we proposed a low power low phase noise ring-VCO based frequency synthesizer with injection locking technique for reducing phase noise. The output phase noise at 3.5 and 10 MHz offset is -116 and -118 dBc/Hz, respectively, and total frequency synthesizer has 6.1 mW power consumption. This circuit was simulated by ADS and its proper behavior was confirmed at technology corners.

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References

1. Sang yeop Lee, Shuhei Amakawa, Noboru Ishihara, and Kazuya Masu, "Low-Phase-Noise Wide-Frequency-Range Ring-VCO-Based Scalable PLL with Subharmonic Injection Locking in 0.18 μm CMOS", Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International.
2. Sang-yeop Lee, Hiroyuki Ito, Shuhei Amakawa, Satoru Tanoi, Noboru Ishihara, and Kazuya Masu, "1.2–17.6 GHz Ring-Oscillator-Based Phase-Locked Loop with Injection Locking in 65nm Complementary Metal Oxide Semiconductor", Japanese Journal of Applied Physics, Volume 51, Issue 2, pp. 02BE03-02BE03-7 (2012).
3. Robert Adler, "A study of locking phenomena in oscillators," Proc. IEEE, vol. 61, pp. 1380–1385, Oct. 1973.
4. Behzad Razavi, "A study of injection locking and pulling in oscillators", Solid State Circuits, IEEE Journal of, volume 39, pages 1415 – 1424, Sept. 2004.
5. Sang-yeop Lee, Shuhei Amakawa, Noboru Ishihara, and Kazuya Masu, "2.4–10 GHz Low-Noise Injection-Locked Ring Voltage Controlled Oscillator in 90nm Complementary Metal Oxide Semiconductor", Japanese Journal of Applied Physics, Volume 50, Issue 2, pp. 04DE03 (5 pages) (2011).
6. X. Zhang, X. Zhou, and S. Daryoush, "A theoretical and experimental study of the noise behavior of subharmonically injection locked local oscillators", volume 40, pages 895-902, May 1992.
7. Behzad Razavi, "RF Microelectronics", (2nd Edition), Prentice Hall Communications Engineering and Emerging Technologies Series, 2012.
8. Jri Lee, Huaide Wang, "Study of Subharmonically Injection-Locked PLLs", Solid-State Circuits, IEEE Journal of, volume 44, pages 1539 – 1553, May 2009.
9. Sang yeop Lee, Shuhei Amakawa, Noboru Ishihara, Kazuya Masu, "Low-Phase-Noise Wide-Frequency-Range Differential Ring-VCO with Non-Integral Subharmonic Locking in 0.18 μm CMOS", Proceedings of the 5th European Microwave Integrated Circuits Conference, September 2010, pages 464-467.
10. Changzhi Li, Jenshan Lin, "A 1–9 GHz Linear-Wide-Tuning-Range Quadrature Ring Oscillator in 130 nm CMOS for Non-Contact Vital Sign Radar Application", IEEE Microwave and Wireless Components Letters, vol. 20, no.1, January 2010.
11. Sang yeop Lee, Shuhei Amakawa, Noboru Ishihara, Kazuya Masu, "High-Frequency Half-Integral Subharmonic Locked Ring-VCO-Based Scalable PLL in 90 nm CMOS", Microwave Conference Proceedings (APMC), 2010 Asia-Pacific, pages 586 – 589.
12. Jinbao Lan, Yuxin Wang, Lintao Liu and Ruzhang Li, "A Nonlinear Phase Frequency Detector with Zero Blind Zone for Fast-Locking Phase-Locked Loops", Anti-Counterfeiting Security and Identification in Communication (ASID), 2010 International Conference on, pages 41-44.
13. Ali Sahafi, Jafar Sobhi, Mahdi Sahafi, and Omid Farhanieh, "An Ultra Low Power Frequency Divider for 2.4GHz Zigbee Frequency Synthesizer", Electrical and Electronics Engineering (ELECO), 2011 7th International Conference on, pages II-234 - II-236.
14. Yeung Bun Choi, Xiaojun Yuan, "A 3.5-mW 2.45-GHz Frequency Synthesizer in 0.18 μm CMOS", IEEE International Symposium on Radio-Frequency Integration Technology, 2009, pages 187-190.
15. Zhiqun Li, Yawei Jiang, Haiyong Shu, Ningbing Hou, "A 5-GHz Frequency Synthesizer with AFC for Low IF ZigBee Transceiver Applications", New Circuits and Systems Conference (NEWCAS), 2011 IEEE 9th International, 26-29 June 2011, pages 530-533.
16. Debashis Mandal, T. K. Bhattacharyya, "7.95mW 2.4GHz Fully-Integrated CMOS Integer N Frequency Synthesizer", 20th International Conference on VLSI Design (VLSID'07), 2007.