Providing a New Architecture for Network on Chip

Mohammad Sohrabi[1,*], Masoud Katiraee[2]

[1.] Department of Computer Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran
[*]Email: st_sohrabi@azad.ac.ir
[2.] Department of Computer Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran
Email: m_katiraee@azad.ac.ir

ABSTRACT: The idea of "network on chip" or "NOC" has been taken from distributed systems and computer networks with the purpose of structured and scalable connection of chip components. Most of the ideas existing in the above mentioned domains applying the limitations of this application have been given way to this domain as well. In the present study, a new topology has been presented for the "NOCs", which is the modified topology of the diagonal mesh typology for utilization in the domain of "NOC". The proposed topology has been both investigated and compared with mesh topology. The presented architecture based on this topology has been simulated using the "OPNET" software and its performance and delay have been compared to those of the architecture equivalent to mesh topology. It has been shown that this network has a higher performance and lower delay compared to mesh network.

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1. introduction

"System on chip" design methodologies have undergone significant modifications over recent years. According to Moore's law, the processing resources on the chip double every year. The speed of the technological advancement has been a little less than this prophecy and for a constant chip size, it doubles every three years. According to this law and the presented papers, the possibility of having a large set of processors hidden in a system design on a chip is inevitable. The main component in such platforms, multiprocessor "system on chip", is the typology of internal connections. Such structures imply an integrated accumulation of components with various working frequencies which perform different operations. Integration of different components in a system has led to the emergence of a new challenge, in such a way that infrastructure IP development for the systematic integration of the applied components to widely use "system on chip" design methodology has become a vital issue.

One of the main problems in designing the future generation "system on chip" is rooted in the underdevelopment of the global wires delay. Global wires transfer signals on the surface of the cheap, but their delay improvement has not kept up with the advancement of technology. Although gate delay reduces as the technology advances, global wire delay increases exponentially or linearly in best-case scenario even when buffers are used. Even when buffers are used, the delay of these wires may exceed one clock cycle and require several clock cycles. In ultra-deep submicron processes, at least 80 percent of the critical path delay is due to the internal connections.

Most solutions proposed in 90s for the "system on chip" communication structure were based upon custom design and ad hoc combination of direct system and bus among modules. The exclusive wiring between modules is conducted in terms of band width allocation, delay and the optimized power consumption. The number of links required for module connection increases exponentially with the number of components. So, the problems of area overflow and routing feasibility will begin to show themselves. Consequently, communication structure designing based on direct wiring is not capable of much development and will bring about limitations in terms of increasing the constitutive components.

The dilemma of common media based on arbitrary, like bus, has somehow solved the underdevelopment problem of exclusive wiring. Although using this architecture has somehow solved the development problem compared to exclusive wiring, it nevertheless underscores the system's efficiency for various reasons. First, using a common media will result in having only one connection at the time in the chip and the other components will have to wait until the transfer is over. Second, relatively long communication buses have high resistance and noise capacitor capacity, and as the number of components goes up, so does the capacity of noise capacitor. The overall process reduces the efficiency and the working frequency of bus. Finally, as the wire grows longer, the circuit size grows and so does the power consumption. To solve this flaw and

reducing the limitations, ideas like the pipe line characteristics and hierarchical structure have been proposed. Yet, even such ideas cannot keep up with the technological advancements and the increasing number of components in system design on the chip.

Inspired by computer networks, the idea of "Network on chip" was proposed to solve the aforementioned problems. "Network on chip" strategy can be considered as the mediocrity of the classical network strategies and the special switching and communication strategies for parallel processing. Classical networks are capable of development and have the necessary flexibility to adapt themselves with the general communication patterns. On the other hand, the communication strategies and special switching for parallel processing have the appropriate performance, yet they show limited development capability and weak flexibility in dynamic configurations. The main goal and idea of "network on chip" is to come up with a solution for simultaneous access to performance, development capability and flexibility in the world of SOC's. This problem has led to a proposal for utilizing micro grids with closed switching based on the appropriate communication protocol.

After this idea has been proposed, many groups set out to study and develop this idea. The researchers conducted in this area can be classified as follows:

1) Systematic level (design and abstraction methodology, area of architecture and traffic properties)
2) Network medium (performances and sockets)
3) Network (typology, protocol, current control and service quality)
4) Link level (concurrency, decoding and their reliability).

Based on the above classifications, this research can be considered as belonging to the third level.

In this research, we will first study those researches conducted in the past. Then, the presented typology will be studied and the appropriate path finding algorithm will be presented. Different parameters of the architecture will be presented in next part and then, by determining the simulation scenario, the presented architecture will be compared against the architecture equal to its typology. Finally, the presented architecture results will be discussed.

2. Previous researches

Various essays have been published about network on chip some of which have discussed the details of the presented architecture, while others have explored the generalities of architecture without making any reference to the way they have to be implemented. In the most general sense, the typology used in theses architectures can be divided to regular and irregular groups.

Most architecture proposed for network on chip have been implemented on ring typologies, two dimensional mesh, Torus, tree and customized typologies. Greiner et al. have proposed a general connection sample for networks on chip based on closed switching: SPIN that uses fat tree typology, wormhole switching, adaptive routing, and credit tied current control in this architecture. The network size in this typology increases following the (N log N)/8 pattern. Dally proposes an architecture based on Torus typology that uses circular switching, deterministic routing and virtual channel current control. Kumar et al propose the CHLICHE architecture. This architecture is based on the two-dimensional mesh. Mesh typology was chosen mainly because it is easy to implement on the chip, and simple routing algorithms have been proposed for it. Cesar et al have proposed a developable architecture based on parametric routers and called it SoCIN. This architecture also utilizes two-dimensional mesh typology and XY routing algorithm. Architectures proposed by Liang et al., aSoC, Bolotin et al. group, QNoC, and Wiklund et al., SoCBUS have also used two dimensional mesh typology to connect nodes. Octagon is based on the octal diagonal ring of the nodes, in which every node degree is three. Wormhole switching and deterministic routing have been used in this architecture.

Considering the typologies used on network on chip, it has been observed that the dominant typology in them is mesh typology as it is easy to implement and its routing algorithms are simple. Diagonal mesh typology is the modified version of mesh typology presented for parallel computers and multicomputer. Rather than having vertical and horizontal connections, nodes have diagonal connections in this typology. Tang et al. have proposed this typology along with appropriate routing for it to be used in the field of multicomputer. This typology has been compared against mesh typology, and network diameter has been shown to be less than common mesh typology.

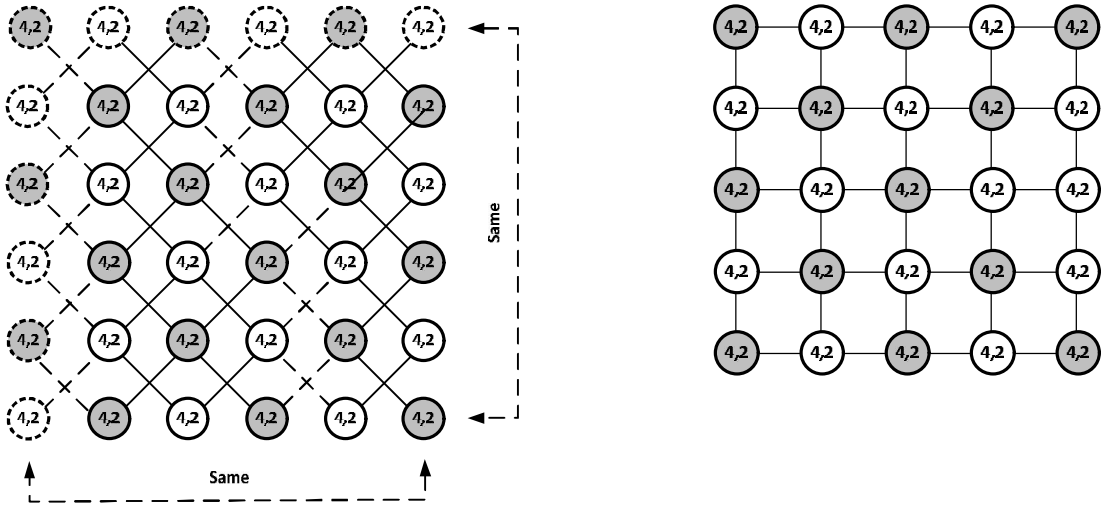
Due to the existence of long links which connected borderline nodes, using this typology without making modifications in the area of network in chip is not appropriate and it has been used in no network on chip architecture. Another limitation of this typology is the network size. The both dimensions of network's size should not be even due to its nature, because two separate networks might be produced.

A new typology based on the diagonal mesh typology has been designed in this paper and the

appropriate routing algorithm for it has been proposed. The new architecture for network on chip has been introduced based on this typology.

3. Introducing the proposed typology

The proposed typology is a mixture of mesh typology and diagonal mesh typology. In mesh typology, vertical and horizontal communication links connect nodes to one another (figure 1a), while in diagonal mesh typology, diagonal links connect network nodes and borderline nodes are neighbors to one another as it is shown in the figure 1b, and long links are used to connect them to each other.



a b

Figure 1: a) Mesh typology, b) diagonal mesh typology

The proposed typology can be observed in figure (2) whose nodes have been labeled by Cartesian features. For every node with such features:

$$(x,y), x \in \left\{-\frac{K-1}{2},\dots,\frac{K-1}{2}\right\}, y \in \left\{-\frac{n-1}{2},\dots,\frac{n-1}{2}\right\} \quad (1)$$

Connections will be defined as:

$$(x,y) \sim \begin{matrix} (\langle x+1\rangle_k, \langle y+1\rangle_n), & (\langle x+1\rangle_k, \langle y-1\rangle_n), \\ (\langle x-1\rangle_k, \langle y+1\rangle_n), & (\langle x-1\rangle_k, \langle y-1\rangle_n), \end{matrix} \quad (2)$$

In which ~ shows the connection and $\langle X\rangle_n$ equals:

$$\langle x\rangle_n = \begin{cases} x & \text{if } |x| \le \frac{n-1}{2} \text{ and Odd n} \\ & \text{if } -\frac{n-2}{2} \le x \le \frac{n}{2} \text{ and Even n} \\ x-1 & \text{if } x > \frac{n-1}{2} \text{ and Odd n} \\ & \text{if } x > \frac{n}{2} \text{ and Even n} \\ x+1 & \text{if } x < -\frac{n-1}{2} \text{ and Odd n} \\ & \text{if } x < -\frac{n-2}{2} \text{ and Even n} \end{cases} \quad (3)$$

In this typology, the borderline nodes are connected to each other according to equation 3. The structure of borderline nodes is exactly similar to central nodes, in other words they have diagonal connections. But their typological structure is such that their vertical and horizontal diagonals are connected to other central nodes in vertical and horizontal manners (figure 2). Corner nodes in this typology have three communicating links and, thus, 3 neighbors. According to equation (2), every node, except for corner nodes, has 4 neighbors, and in the case of corner nodes in equation (3), a link will be established from that nod to itself. As there is not any ring from a node to itself in the network of no link, we will simply ignore this link. Figure (2) shows an N=6*5 network of the proposed typology.

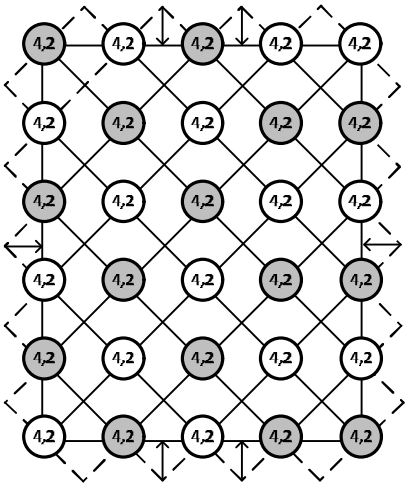


Figure 2: an N=6*5 network 1

Diagonal mesh typology (figure 1b) has some shortcomings that render it inappropriate to be used in the field of network on chip:

- As it has been assumed above in the definition of this typology, both sides of the network have to be odd, because if both sides of the network are even, we will then have 2 separate networks. This problem is one of the limitations for this typology.
- The second problem is the existence of long communication nodes for borderline nodes. The length of these links has is directly related to the size of network and it will contribute to expanding the network size. This problem will render this typology incapable of development for network on chip.

In this respect, the proposed typology doesn't have the problems of diagonal mesh network. The sizes of this typology are quite arbitrary. Also, the communication links size has nothing to do with the network size. On the other hand, while diagonal mesh typology retains the simplicity of mesh typology for implementing on chip, it will display a shorter network diagonal compared to mesh typology.

Network diagonal is the utmost minimum distance between 2 arbitrary nodes in the network. The average delay in network is directly dependent upon network diagonal. Network diagonal in common mesh network with N=n*k nodes is calculated by equation (4) and this is the distance between the nodes on the corners of network.

$$D = (n-1)+(k-1) = (n+k)-2 \quad (4)$$

Network diagonal in the proposed typology is the distance between nodes in the corners of network. Network diagonal for a N=n*k equals:

$$D = (\min\{n,k\} - 1 + |n-k| \quad (5)$$

If network has the shape of square (n=k), the network diagonal will equal n-1 (or k-1) and it is in fact the distance between nodes on the corners of network. Due to diagonal links, this distance equals n-1 as it is shown in equation (5). Now that the totality of problem is established, let's assume n>k. So, we can assume a square network with k*k size in this network. To calculate network diagonal which is the distance between 2 nodes on the corners of the network, all we have to do is to add k*k square network diagonal with corner node distance in k*k network and corner node in k*k network. As corner nodes in both networks are among border nodes, there are vertical and horizontal links among them. Thus, distance between these 2 nodes equals n-k. According to the above mentioned equation, network diagonal in k*k network equals k-1, and in general terms, network diagonal equals (k-1)+(n-k).

4. Routing

A crucial issue in designing network on chip is to choose the routing algorithm in network. Routing issue can be defined as determining a route for packages to go from the beginning point to the final destination. In fact, this issue greatly influences network's performance and power consumption. Moreover, more complex routings will lead to larger designs. So, the routing issue is a balance between performance and the area. To propose a routing algorithm for every network, first we need to clarify network nodes to have easy access to them. In this section, we will explore ways for presenting nodes' coordinates and an algorithm for routing.

4.1. Coordinate system and nodes' coordinates

To present an independent and label determined routing algorithm, the coordinate system shown in [13] has been used. In this coordinate system, the common coordinate axis of X & Y have turned counterclockwise for 45 degrees and extended for $\sqrt{2}$. In other words, a coordinate system suitable for diagonal connections was prepared.

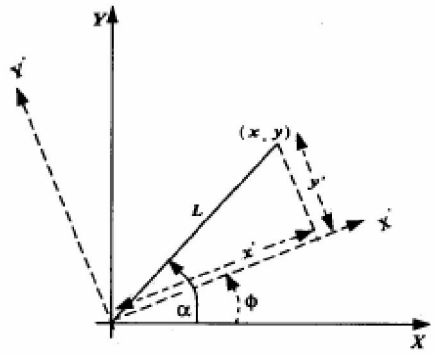


Figure 3: moving node labels among coordinate systems [13]

This coordinate system can be formulized as follows:

In figure (3), coordinate axes X-Y have turned counterclockwise for ϕ degrees to form $X'-Y'$ axes. For a specified point of (x,y) in X-Y coordinate system, we have:

$$x = L\cos\alpha \quad (6)$$
$$y = L\sin\alpha$$

L and α are respectively the length and the angle of that point (figure 3). The coordinate of this point in the new $X'-Y'$ coordinate axes is as follows:

(7)

$$X' = L\cos(\alpha - \emptyset)$$
$$= L\cos\alpha\ \cos\emptyset + L\ \sin\alpha\sin\emptyset$$
$$= x\cos\emptyset\ +\ y\sin\emptyset$$
$$y' = L\sin(\alpha - \emptyset)$$
$$- L\sin\alpha\cos\emptyset - L\cos\alpha\sin\emptyset$$
$$= -x\ \sin\emptyset + y\cos\emptyset$$

In this case, $\phi = 45$ and X & Y axes have to be extended for $\sqrt{2}$. So, the transfer result will be like equation (8):

$$x' = \sqrt{2}(x\cos 45^{\circ} + y\sin 45)$$
$$= x + y$$
$$y' = \sqrt{2}(-x\sin 45^{\circ} + y\cos 45) \quad (8)$$
$$= x + y$$

So, every point with (x,y) coordinates in X-Y coordinate system will have a label like (x', y') in the new coordinate system where x' and y' will be determined by equation (8). Labeling a 5*5 network nodes can be observed in figure (4).

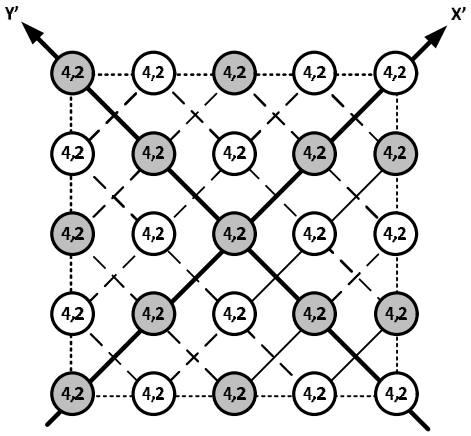


Figure 4: labeling a 5*5 network in new coordinate system

4.2. routing algorithm

As we have just noted, network nodes in the new coordinate system are labeled. If we look closely at figure (4), we will see that nodes, regardless of vertical and horizontal connecting links for central nodes, form 2 completely separate networks, where there is no connection between them except for the vertical and horizontal nodes.

Labeling nodes in this new coordinate system is such that not only does that show their position in the network, but it also determines which of these 2 separate networks they belong to. Considering the node features in any of these networks, we see all nodes of a network have odd x & y, and all nodes of other networks have even x & y. Thus, oddness or evenness of every node determines that node's network. So, there are 2 ways to determine nodes network in routing algorithm:

1) By performing process operations and in terms of destination node address, central nodes determine the network of that node.
2) In terms of destination node address, the starting node determines its network. There is a field in the header of packages which determines destination network and its value is determined by the sender.

Second method, the excessive overload is applied to the header of packages, yet the process load in routers is just limited to checking a field in the header of package. As only one bit is added to the header of packages in this method, choosing the second method seems to be the best way.

On the other hand, any of these 2 separate networks, regardless of how the nodes are connected to one another, forms a simple mesh network itself whose routing algorithms can be used here as well. One of the simplest yet most applied routing algorithms is X-Y routing algorithm. In this paper, a two-stage routing algorithm based on the same algorithm will be proposed.

As we can see in figure (4), every node, except for central nodes, have five connections to north east, North West, south west, south east and a local connection. If both source and destination nodes belong to the same network, then routing method will be just like that of X-Y, i.e. packages are first routed along X' axis and then along Y' axis towards destination node.

When source and destination nodes are not located in a single network, routing algorithm will be a little different. As the 2 networks' connection can only be established through central nodes and vertical and horizontal links, the only thing we have to do is to get the packages to appropriate borderline nodes in terms of destination address and source router address. Then, the network has to be changed on those nodes and after this, X-Y routing algorithm for getting a package to its destination will be implemented. Thus, right after packages have entered the network, local router will direct them to the appropriate port.

After receiving every package, central routers will explore its destination node network. If the package's destination node belongs to the same network that does the router, the package will be routed first along X' and then along Y' axis according to destination address and that router's address. If the package doesn't belong to that router's network, router will send the package to another port in front of the receiving port of that package. For

example, if router has received the package from northwest port yet it doesn't belong to the same network, package will be sent to south east port.

Routing the opposite network's packages in borderline routers is different from central routers, but routing packages from the same network is just like XY routing. Borderline routers are connected to 2 routers from other networks, one of which has a higher y' value and the other one has a lower y' value than the y' of that router. These attributes are used to optimize routing algorithm. In these routers, if the package does not belong to the router's network, routing will be done along y' axis and it will be sent to an appropriate router from another network.

5. Different parameters of architecture

A network architecture is not just limited to it typology and routing algorithm. Different parameters determine the architecture of a network which have to be taken into account while presenting an architecture. These parameters can be thought of as the applied switching mechanism, communicating links size, buffer size, number of virtual channels, and bandwidth allocation among them. In this part, these parameters will be determined for the proposed architecture.

5.1. Switching

One of the issues about routing is the switching mechanism used in the network. Switching technique determines when switching must take place, how the internal switches of routers have to be seated and re-seated, and how packages should be transferred among switches. As a result, fulfilling the applied limitations by the application type using various switching techniques is a balance between implementation (usually area) and performance complexity.

Various switching techniques have been proposed including: store-and-forward, cut-through and wormhole. Among various techniques applied in network, wormhole routing is one of the best for network on chip field since it requires it needs limited buffering resources and precise delay requirements. In this design we have also used wormhole technique.

In this architecture, packages are broken to 32-bit flits which are equal to the size of communicating links. In addition to every package's information, 2 other flits are added to the package which determine the end and the beginning of the package. The overload flit carries information about routing and the coordinates of destination node. Every router, without needing to receive all flits of a package, sends the receiving flits towards destination, if it is possible to send.

To determine the destination of a package's flit, every router has a routing table which is updated right after the flit overload of a package is received and its destination is determined. The route then sends the next flits of that package toward the destination based on her routing table.

5.2. Links' bandwidth and the buffers' size

The bandwidth of network channels is determined as follows:

$$BW = f_{ch} \times w \quad (9)$$

In this equation, f_{ch} is the working frequency of the link, and w represents the width of the link (in wormhole routing, link width shows the size of the flits). The bandwidth issue can also be defined as:

Determining the bandwidth for links so that 1) limitations imposed by application type (power consumption, total wire length, area, etc.) are fulfilled; 2) network delay has to be set in minimum level, and throughput has to be set to the maximum level. A solution to improve the links' bandwidth is to increase communication links width. Yet, it has to be kept in mind that such a thing will have side effects like increasing the area. Apart from the influence of area, choosing w influences the length and distance of wires which in turn determine the working frequency. So, it is impossible to simply optimize bandwidth while independently considering w and f_{ch} .

Choosing channel width in designing network on chip has never been studied and assessed. Dally et al. use 256 bits to exchange information, while current designs of network on chip uses 32-bit channels.

The proposed architecture has also used 32-bit channels. In other words, the flit size in this architecture is 32 bits. Buffer size in designing network on chip is one of the major design issues. As the buffers of every router increase, so does the overload of the area, and on the other hand, depending on the network's working load, increasing the buffer size can help increase performance power and reduce network delay. Using buffer in the inlet and outlet of every router's ports improves network's performance. Considering all these issues, buffers with the size of 2 have been used in the inlet and outlet of each port.

5.3. Virtual Channels

Virtual channel is one of the mechanisms for controlling the current. Wormhole routing with controlling virtual channel flow is a recognized technique from the field of multiprocessor networks. This mechanism reduces the buffer size and, consequently, area overload and power consumption and helps gain appropriate efficiency from channel.

Router structure for the utilized virtual channel in the proposed architecture is such that it uses four virtual channels for every link. Virtual channels use communication channel in the form of a Round Robin algorithm. As long as the flits related to a package are

available in a virtual channel, the link will be in possession of that virtual channel. As a virtual channel's flits are over or the final flit of a package is delivered, the turn for this channel is over, and another virtual channel which has flit will be chosen in a rotator manner. In this way, the bandwidth of the links will be evenly divided among virtual channels, and all virtual channels will have an equal share of link bandwidth. Of course with this method, network provides only one type of service. To define various system classes we need to design an appropriate algorithm for virtual networks to use communicating links.

5.4. Simulation Scenario

The proposed architecture has been modeled and analyzed using OPNET software. To compare these typologies, two 5*5 networks (one with the proposed typology and one with the common mesh typology) with similar architecture parameters were modeled. Packages have been sent into network with random destination address and in the Burst manner with a constant rate.

5.5. Simulation results

Figure (5) shows the number of packages available in network in terms of time. As it can be seen, the number of available packages in the network after it has been stabilized is much less than mesh network. This is due to shorter distance of nodes in this typology which causes the network to have higher traffic capacity and, consequently, higher performance.

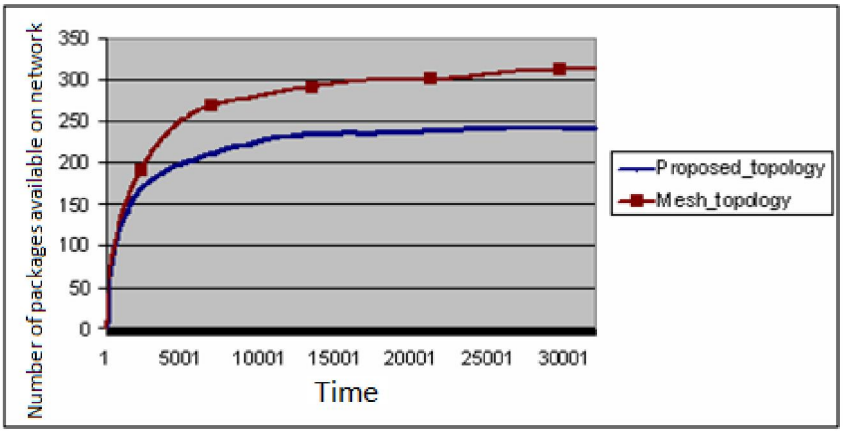


Figure 5: the average package numbers available on network in terms of time

Figure (6) shows the average end to end delay for packages available in network. As we can see, the average delay in the proposed network is much less than mesh network. This demonstrates the shorter average distance for this network than mesh network.

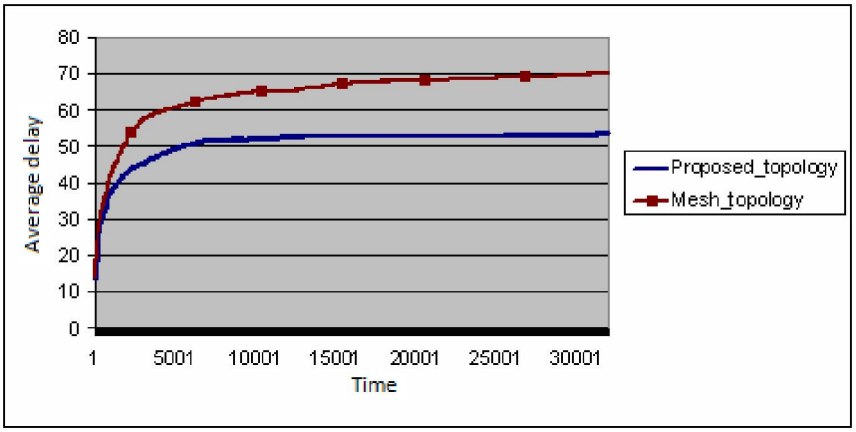


Figure 6: average end to end delay for packages in terms of time

Figure (7) shows the number of packages discarded from network during simulation. These packages were discarded from network due to their congestion. As you can see in the picture, the number of discarded packages in mesh network is more than those in the proposed network. This phenomenon can

be justified in the following way: due to shorter average distance, packages were delivered earlier and, consequently, fewer packages remained in the network. This decreased the probability of elimination and interference between them.

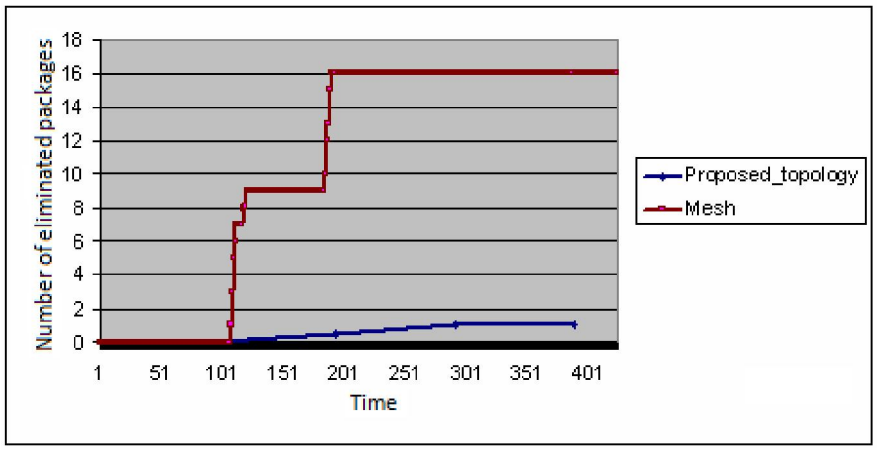


Figure 7: number of eliminated packages from network

6. Conclusion

In this paper, a new typology based on diagonal mesh typology to be used for network on chip field was proposed. Based on this typology, an architecture for network on chip was proposed. The proposed architecture was compared against mesh-typology-based architecture with similar architecture parameters, and it was shown that this typology has higher efficiency and less delay compared to mesh typology. Thus, using this typology in real time applications is preferred to mesh typology.

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