Noise Immune Conditional Footer Domino WIDE-OR Logic Design

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Abstract: In this paper, a novel circuit design idea is proposed for improving the noise immunity of domino logic circuits that are especially useful for wide fan in gates. Leakage current is the most important issue in ultra deep submicron technologies. This is the main motivation for proposing a new idea for decreasing sub-threshold leakage current in domino logic circuits for deep submicron technologies. The proposed circuit design enhances the noise immunity at least by a factor of 2.02X to 8.16X compared with other conventional domino circuits and does not suffer from the disadvantages of our previously proposed design. The proposed circuit design has been simulated using the Predictive Technology Models (PTM) for 70nm CMOS technology. [Journal of American Science 2010;6(10):898-903]. (ISSN: 1545-1003).

Keywords: Domino logic, Noise immunity, wide gates, high performance.

1. Introduction

Dynamic gates are widely used for high performance processors and are also used in full adders that are the most important part of a CPU. Domino logic circuit techniques are widely used compared with CMOS static circuits due to their high performance and area characteristics. The high speed characteristics of domino logic circuits are primarily due to their low noise margin [1-3]. However, this low noise margin increases the sensitivity of domino logic circuits to noise. As the noise margin of domino logic circuits increases with the down-scaling of the manufacturing technology and the increasing of their operational frequency, the error-free operation of domino logic circuits is the most important challenge. The decreased threshold voltage with scaling down the voltage supply increases the speed while it places the power consumption at an acceptable level. However, the decreased threshold voltage decreases the noise immunity because of the increasing sub-threshold leakage current. Sub-threshold leakage current increases exponentially with scaling down of the manufacturing technology especially for UDSM technologies, and the increase in temperature.

The dynamic power due to scaling the supply voltage is controlled, but the static power is increased with the technology scaling if we only scale down the supply voltage of devices. We also have to scale down the threshold voltage; otherwise, the delay will increase significantly. Thus, the decreased threshold voltage exponentially increases the sub-threshold leakage according to the following equation:

$$I_{SUB} = \mu_o C_{OX} (\frac{W}{L}) A e^{q/n'KT (V_{GS} - V_T)} [1 - e^{-V_{DS}(q/KT)}]$$

where W and L are the effective channel width and length, respectively. Moreover, $A=(KT/q)^2 e^{1.8}$. $V_{DSAT}=V_{GS}-V_t$ and $V_t = V_{T_0} + \gamma' V_S - \eta V_{DS}.$, μ_0 is the zero bias mobility, C_{OX} is the gate oxide capacitance per unit area, n' is the sub-threshold swing coefficient for the transistor, and V_{T_0} is the zero bias threshold voltage. The body effect for small values of V_S is nearly linear. It is represented by the term $\gamma' V_S$ where γ' is the linearized body effect coefficient and η is the drain-induced barrier lowering coefficient (DIBL) [6].

As a result, static power will constitute a significant portion of total power dissipation in dynamic logic circuits [4]. It has been shown that the share of static power consumption in gates is increasing rapidly compared with that of dynamic power dissipation as the technology scales down. This static power is mainly due to leakage. Various circuits have been proposed for leakage reduction, increasing the speed or improving performance and robustness simultaneously [5]. Dual-Vt techniques have been proposed in the literature [6-7] and Alvandpour et al. [8] have proposed the conditional keeper logic circuit. A new circuit design technique is proposed in this paper.

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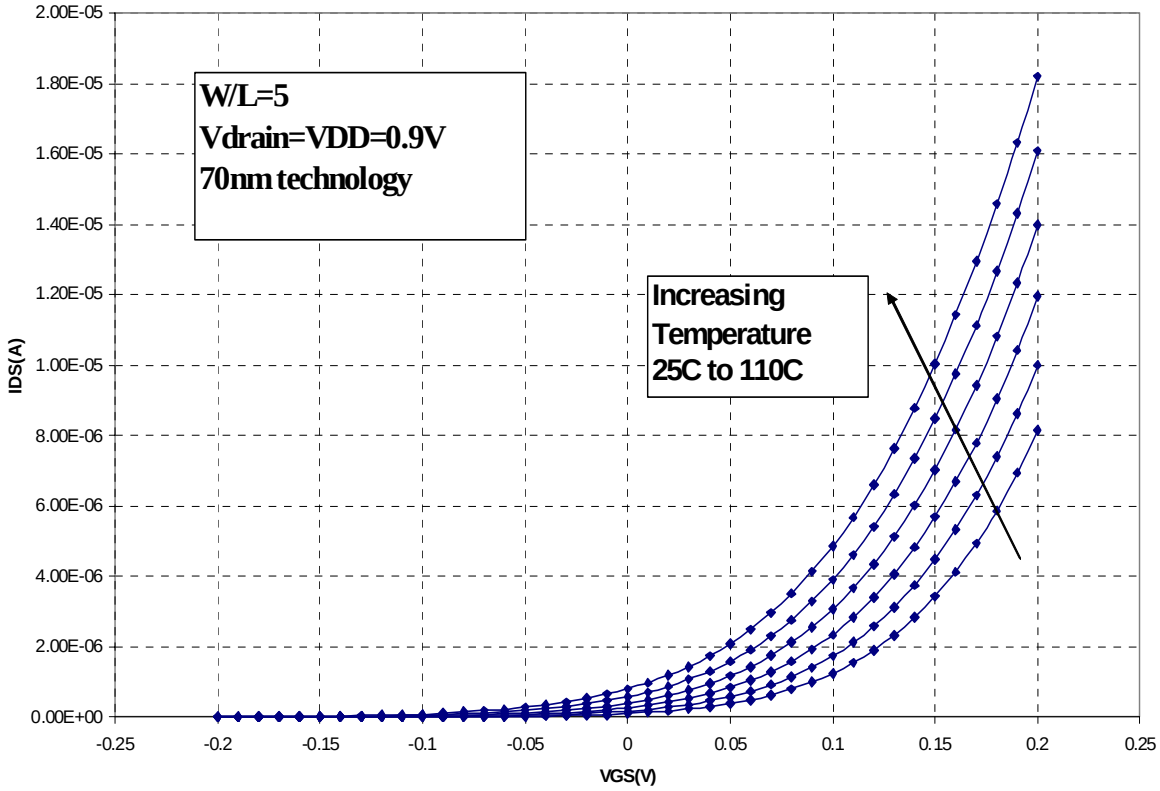

Fig 1: IDS vs. VGS for T=25 to 110C

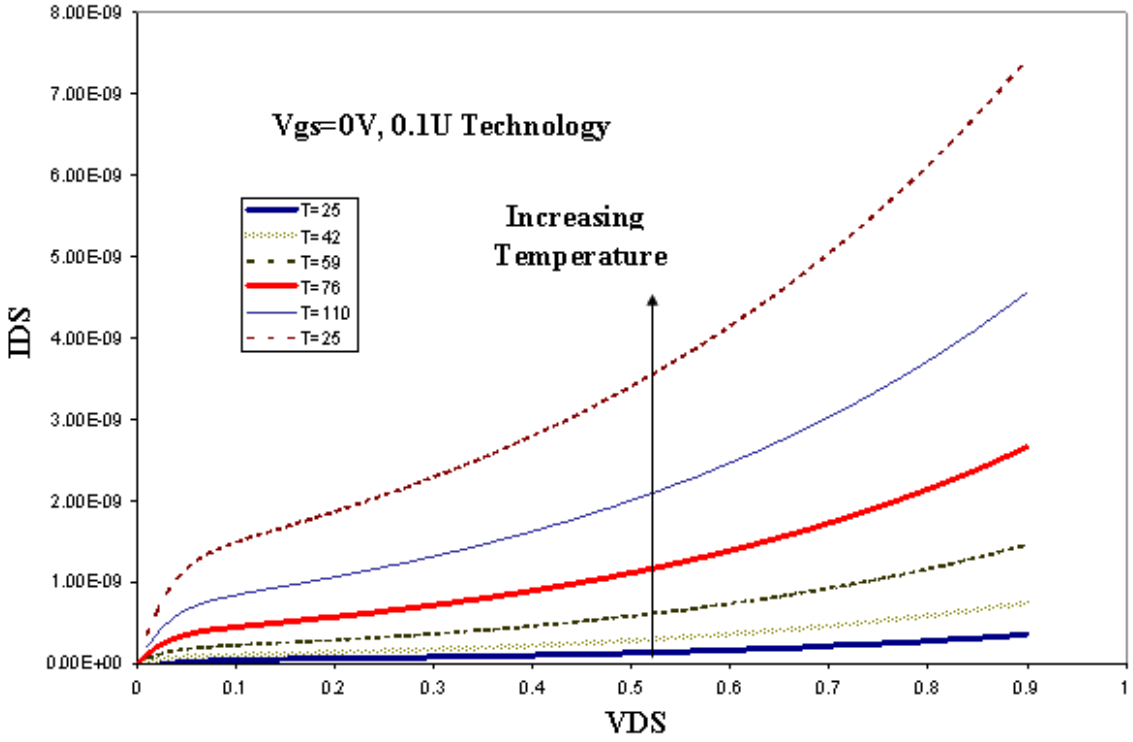

Fig 2: IDS vs. VDS for different temperatures

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The paper is organized as follows: Section II describes dynamic node characteristics and effective items that degrade the waveform of the dynamic node for standard domino logic circuits. The proposed circuit is presented in section III. Simulation results will be presented in section IV. Finally, the conclusions will be presented in the last section.

2. Characteristics of the dynamic node

The main motivation for using dynamic gates in circuit design lies in the fact that they require much less complexity and need much smaller die area. They also have higher speed and use fewer number of transistors that is approximately 50% that of an equivalent circuit in static logic designs. The keeper transistor is used to maintain the state of the dynamic node in the presence of coupling noise, charge sharing and sub-threshold leakage current. The keeper transistor is on in the pre-charge mode. So, it helps charge the dynamic node to VDD. But when the clock is high, i.e. we are in the evaluation phase, the keeper transistor stays on in the primarily time of evaluation phase independent of any input signals applied to the evaluation network. For wide OR gates, the sub-threshold leakage current degrades the dynamic node to such an extent that it may even change its state.

The sub-threshold leakage current increases in a quadratic fashion with increasing temperature as illustrated in Fig. 1. So, for a temperature of $110^{\circ}C$, the leakage current is significantly affected. One of the possible ways for reducing the sub-threshold current is using a heat sink for the circuit. Other parameters that affect the sub-threshold leakage current are threshold voltage and gate-to-source voltage. Unfortunately, scaling down the power supply voltage in order to decrease the dynamic power would increase the delay. Therefore, we have to scale down the threshold voltage too. Scaling down the threshold voltage would significantly increase the sub-threshold leakage current due to the exponential relationship that holds between sub-threshold current and threshold voltage. Also, increasing the voltage of drain to source would increase this current according to the sub-threshold current equation. The effect of power supply variations on sub-threshold current is shown in Fig. 2.

In the standby mode, if the gate to source voltage is decreased the sub-threshold current would decrease significantly. Fig. 1 shows the variations of the sub-threshold current vs. gate to source voltage with voltage of drain equal to VDD. The simulation results are for single NMOS transistor. We can use this point in our circuit designs.

Another factor that degrades the state of the dynamic node is charge sharing. Charge sharing which occurs in any CMOS domino gate may degrade the output voltage level. It may even cause an erroneous output value.

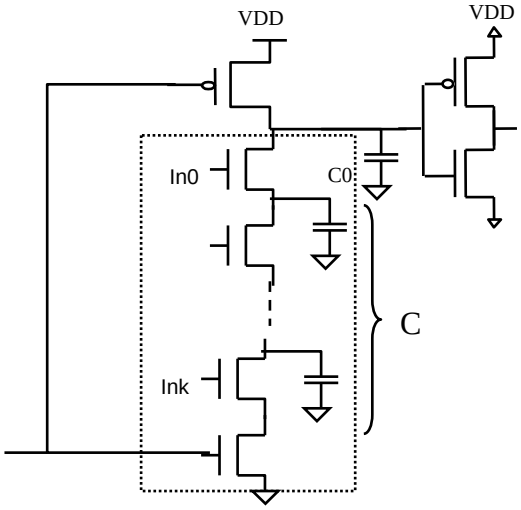

Fig 3: (K+1)-input AND GATE adopted from [9]

As we mentioned before domino gates have two basic phases of operation. They are in the precharge phase when the clock is low and are in the evaluation phase when the clock is high. During the precharge phase, the capacitance C0 will be charged to a high state. During the evaluation phase, if all the inputs Ini are high, the voltage of the dynamic node Vx in Fig. 3 is pulled to ground. Despite several advantages, domino circuits require special care to avoid the charge-sharing problem that may result in erroneous output values. Consider the domino (K-input) AND gate shown in Fig. 3. During the evaluation phase, suppose all inputs Ini are high except for Ink, that is located next to the clocked transistor Mn which is assumed to be low. Since Ink is low, ideally the value of Vx, should remains high. However, the charge in C0 loaded in the precharge phase is shared or redistributed to the (source-drain) junction capacitance of those transistors which are turned on.

Several researchers have attempted to solve the charge sharing problem in domino logic designs [9].

Next, we shall describe the effect called stacking. Leakage current through a stack of two or more "off" transistors is an order of magnitude smaller than a single devise. The stacking effect becomes stronger with technology scaling-down while DIBL (Drain Induced Barrel Lowering) worsens. Many circuit blocks in a microprocessor already contain a significant number of transistor stacks in complex logic gates. Thus, there can be a reduction in leakage power by activating the "minimum leakage" input vector during the idle mode. A two-fold reduction in standby leakage power is achievable for a 32-bit adder.

In addition, transistors that are not performance-critical can be converted into stacks to reduce leakage without any impact on the overall processor performance. Thus, forcing stack allows us to emulate the behavior of high-VT devices that are not available in the process technology. Using, a simple-V_T process in conjunction with "stack forcing" can reduce leakage power of a 32-bit instruction decoder block by 3X without any performance degradation [10-12].

Peiravi et al. [13] proposed a novel conditional footer domino logic circuit that used a current source to maintain the output state during static conditions. The proposed logic circuit provided for better noise immunity, reduced leakage current and considerable reduction of static power consumption.

In this paper, an improved version of the conditional footer domino novel circuit design is proposed. The present design for domino logic helps the circuits to become tolerant to sources of noise. We call this improved conditional footer logic (ICFL). The proposed circuit improves both the robustness and the leakage tolerance of high fan-in domino gates. This techniques uses a smaller keeper transistor that results in less contention between keeper and evaluation transistors. The improved conditional footer domino logic results in a lesser gain in noise immunity compared with the previously proposed conditional footer domino. Although the new logic has added small size transistors in the foot logic compared to our previously proposed logic [13], there is an overall die area reduction since it no longer requires the current mirror that may suffer from excessive die area consumption and mismatch problems.

We have simulated our circuits in HSPICE using the Predictive Models (PTM) for 70nm CMOS technology [14].

The rest of the paper describes the proposed circuit and compares it with conventional domino logic styles for wide OR gates since they constitute a major circuit element in many digital designs. We have used an existing metric for noise (leakage) immunity. It is used to compare the UNG of different circuit styles [1].

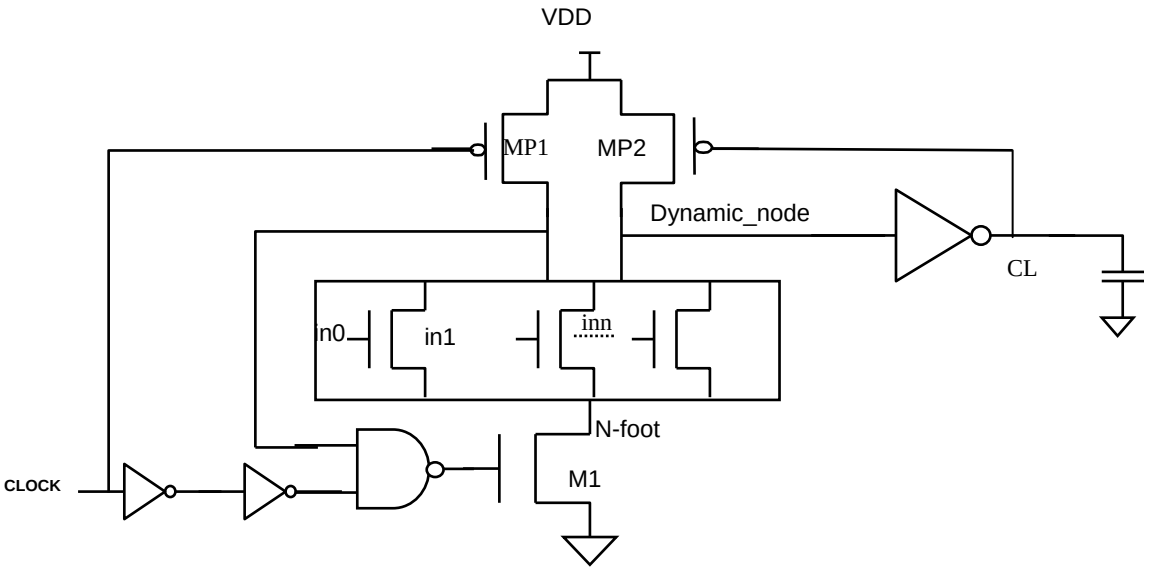

Fig 4. The proposed WIDE-OR ICFL circuit

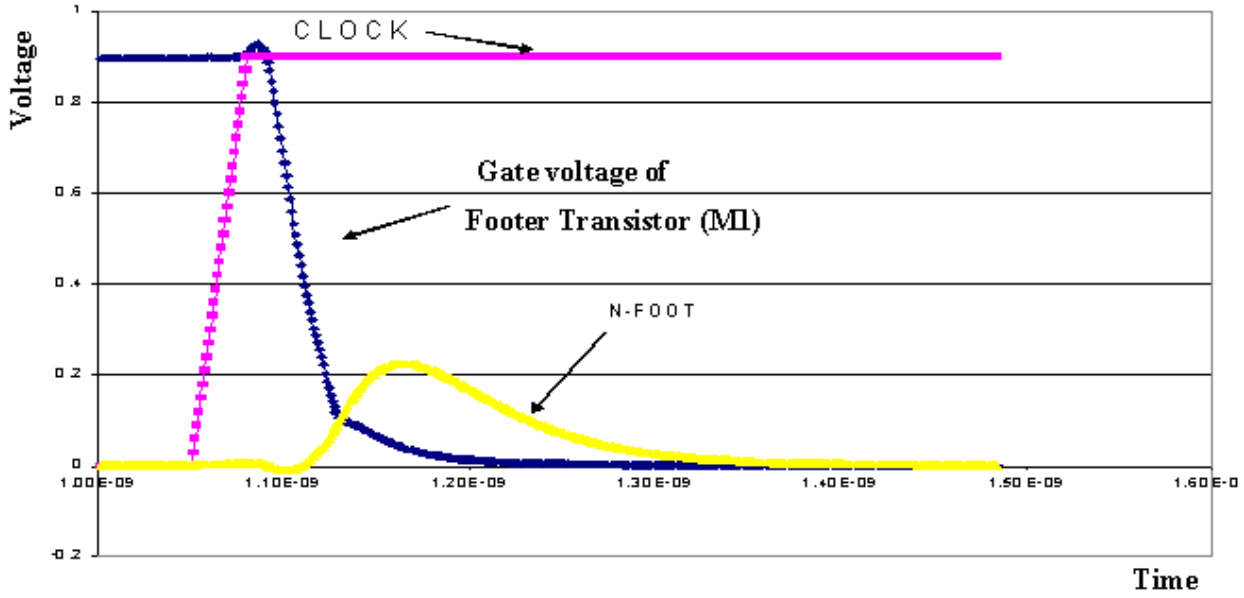

Fig 5: Waveforms of ICFL

3. The Proposed Circuit

Next let us present a new domino logic circuit called conditional footer logic (ICFL) as illustrated in Fig. 4. This circuit works as follows. When clock is low, the circuit is in the precharge phase like a conventional domino circuit. In the precharge mode, MP1 is turned on. Therefore, the dynamic node starts to charge to VDD. After a small delay, the keeper transistor is turned on and helps achieve a faster transition from low to high in the dynamic node. Now, what happens to the circuitry added to conventional domino circuit? The dynamic node is high, and the clock is low. Thererefore, the gate voltage of MN1 is high. This causes N_foot node to be connected to ground. But, in the evaluation phase when the clock is high the dynamic node maintains its previous state (e.g. high) if all the inputs to the evaluation transistors are low.

So, after the delays for inverters, both inputs to NAND gate are high. Then after the delay for the NAND gate, the gate voltage of MN1 goes low and then MN1 is turned off. This behavior can be seen in Fig. 5. But if just one input to the evaluation network is high, the voltage of gate of MN1 remains high and MN1 stays on. The noise immunity of ICFL is improved compared with conventional styles as seen from the results indicated in Table 1.

We have simulated the proposed circuit using the predictive model for 70nm CMOS technology, in bottleneck temperature (T=110C). The simulation for 8, 16, 32, 64 OR gates have been carried out with HSPICE. The results for CFL have been listed in Table.1.

We have also compared the UNG of CFL in same delay condition with other conventional domino logic circuit. The UNG of the proposed CFL circuit has improved from 2X to 8.1X for fan in of 8 to 64. Noise immunity can be improved even further by upsizing delay inverters and the keeper transistor [13].

Table1: Comparison of UNG under similar conditions of delay (ICFL=improved conditional footer logic, FLSDL=footless standard domino logic)

Fan-in	FLSDL	ICFL	Improvement
8	0.17	0.345	2.02X
16	0.13	0.292	2.24X
32	0.09	0.275	3.05X
64	0.03	0.245	8.16X

4. Conclusions

In this study, an improved conditional footer domino logic circuit design style is proposed that has somewhat lower noise immunity compared with the Conditional Footer Logic (CFL) that we proposed earlier. However, this circuit improves noise immunity, has an acceptable performance for high fan-in gates compared to conventional domino logic styles, and does not suffer from the potential problems of the mirror circuit in the previous design. Our proposed circuit enables robust use of high fan-in domino gates in scaled ultra deep submicron technology.

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