A Complete General Logic-Based Intelligent Approach for HIF Detection and Classification in Distribution Systems

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Abstract: The High Impedance Faults (HIFs) are the faults which are difficult to detect by overcurrent protection relays. In this paper a general logic-based intelligent approach for detecting and classifying the HIF in distribution systems is presented. The proposed approach recognizes the distortion of the current waveforms caused by the arc usually associated with HIF. The Discrete Wavelet Transform (DWT) based pattern recognition is used for extracting the current signals. Single line to ground, double line to ground, and three lines to ground faults are classified using three simple logic functions. In order to detect the faulty feeder a general logic-based intelligent approach has been designed. The proposed approach is verified by applying several fault scenarios on IEEE-34 node test system. The proposed approach can be applied for any configuration, current rating or voltage rating. The results confirm that the proposed approach accurately detects and classifies the HIF in the distribution systems.
[Ebrahim A. Badran, Elsaeed Abdallah, and Kamal M. Shebl. **A Complete General Logic-Based Intelligent Approach for HIF Detection and Classification in Distribution Systems.** Journal of American Science 2011; 7(10):320-328]. (ISSN: 1545-1003). http://www.americanscience.org

Keywords: Fault Detection, Fault Classification, HIF, DWT, Distribution Systems

Introduction

Detection of high impedance faults (HIF) still presents important and unsolved protection problem, especially in distribution networks [1]. This type of faults usually occurs when a conductor touches the branches of a tree having high impedance or when a broken conductor touches the ground. In the case of an over-current relay, the low levels of current associated with HIF are below the sensitivity settings of the relay [2].

In recent years, many researchers represented various techniques in HIF detection. The application of Artificial Neural Networks (ANN) based algorithm for HIF detection in multi-grounded medium-voltage (MV) networks is presented in [3], where two signals are used to detect HIF in the system through the power calculation. An intelligent approach for HIF detection in power distribution feeders using Probabilistic Neural Network (PNN) and Forward Neural Network (FNN) is used in [4]. This approach uses the harmonic components of fault currents during HIF as an input to an Estimated Kalman Filter. In [5] an approach to protect the radial power system against faulty conditions using fuzzy-logic scheme is introduced. In this approach the signals of both voltage and current are used for detection.

In [6] and [7] the Nearest Neighbour Rule (NNR) is used for determining the fault or non-fault situations, where the rms values of both voltage and current in various frequency bands are used to recognize the fault. In [8] the measured phase current waveforms for different feeders in MV are used to detect HIF. A fault detection and classification algorithms that captures the current signals in the high voltage transmission system under HIF at one end depending on logic functions is introduced in [9]. An intelligent technique for HIF detection using combined Extended Kalman Filter (EKF) and Support Vector Machine (SVM) have been used in [10]. This technique uses the magnitude and phase change of fundamental and sub-harmonics components as an input to SVM.

In most of the above approaches the signals of the feeder current have been used to HIF detection. Discrete Wavelet Transform (DWT) method has been used to extract the current signals into two frequency bands. Therefore, DWT is an appropriate tool in analysis of HIF detection [6-9].

In this paper a general logic-based intelligent detection and classification approach is proposed. It involves capturing the current signals generated in distribution lines of the system under HIF. The proposed approach has been aimed to intelligence classification between the various faults types and the faulty feeder using a simple methodology.

1. Fault Detection Algorithm

Wavelets are families of functions generated from one single function, called the mother wavelet [8]. Scaling and translating operations are applied using the mother wavelet on the analyzed function. The scaling operation is used to dilate and compress the mother wavelet to obtain the respective high and low frequency information of the analyzed function. Then, the translation is used to obtain the time information. In this way a family of scaled and translated wavelets is created and it serves as the base for representing the analyzed function. The DWT is represented in the form:

$$DWT(m,k) = \frac{1}{\sqrt{a_0^m}} \sum_n x(n)\, \psi(\frac{k - nb_o a_0^m}{a_0^m}) \quad (1)$$

where *x(n)* is the analyzed function, the mother wavelet ψ is discretely dilated by the scale parameter a_0^m and translated using the translation parameter $nb_o a_0^m$, where a_o and b_o are fixed values with $a_o>1$ and $b_o> 0$, and *m* and *n* are integers. By selecting $a_0=2$ and $b_0=1$, the DWT is implemented using a multistage filter. The mother wavelet is used as a low-pass filter and its dual as a high-pass filter.

Several wavelet families were tested to extract the fault features using the Wavelet toolbox incorporated into the MATLAB program. Daubechies wavelet 14 (db14) is appropriated for localizing this fault [11].

The proposed algorithm uses the DWT for HIF detection. The strategy of the fault detection is arranged as shown in Fig. 1. At the measuring node of each feeder, the phase currents are measured and extracted using DWT. The absolute sum of the third details (d3) coefficients for three phases is computed (S_{Ia}, S_{Ib}, and S_{Ic}). The decision logic is designed such that S_{Ia}, S_{Ib}, or S_{Ic} must stay above a magnitude of a threshold level, S_{th}, for tripping condition. The setting value of this threshold is depended on the distribution system operating parameters. The threshold level is selected according to the maximum normal operating current in the system.

In order to classify between the different fault types; single line to ground (SLG), double line to ground (DLG), and three phases to ground fault (3LG), a three logic functions are designed. The inputs to the three logic functions are the absolute sum of the details coefficients for each feeder. The absolute sum value of the third detail (d3) over one power cycle is computed in a discrete form at each measuring node. This absolute sum is represented by [8]:

$$S_I(n) = \sum_{K=n-N+1}^{n} |d3_I(K)| \quad (2)$$

where *K* is used for carrying out a sliding window covering 20 *ms* and *N* is a number of window samples. Fig. 2 illustrates the designed three logic functions which are used to classify between SLG fault, DLG fault, and 3LG fault. The input to the three logic functions are S_{Ia}, S_{Ib}, and S_{Ic} while, T is the detection decision. The detection decision value is "1" when the HIF exists and "0" otherwise. A general approach is designed for detecting the faulty feeder, as shown in Fig. 3.

The inputs to the proposed approach are the absolute sum of the wavelet details for each phase of all feeders. The difference between the absolute sum for each two feeder at the same phase is computed. After calculating all difference between feeders the generalized logic function can be identified the faulty feeder between all feeders in the system.

3. The Proposed Approach Verification

A benchmark distribution system is used to validate the proposed HIF detection and classification approach. The IEEE-34 node test system, shown in Fig. 4, is selected for this purpose. The HIF arc model used in this analysis to represent the arc resistance is picked from [12]. The HIF arc model is implemented at node 842, which represents a three-phase unbalance load. The three types of faults are applied; SLG fault, DLG fault, and 3LG fault. The current of all feeders are extracted using DWT. Then, the proposed approach is carried out.

3.1 Single Line To Ground Fault (SLG)

A SLG fault is implemented on node 842 at phase a. Fig. 5 illustrates the absolute sum of d3 for all feeders in the system. It is shown that the S_{Ia} is higher than S_{Ib} and S_{Ic} in all feeders. Also, it is noted that S_{Ia} is higher than the threshold value in all feeders. Therefore, the proposed detector detects successfully the faulted phase (i.e. phase a).

Fig. 6 demonstrates the classification logic output. It is shown that, phase a in all feeders have a logic output of "1" at arc fault instant. In order to find out the faulty feeder the general technique has been applied for five feeders. The output of this technique for SLG fault at phase a is shown in Fig.7. it can be seen that feeder 3 have a logic output of "1" at arc fault instant. Therefore, the detected fault is SLG at phase a of feeder 3.

3.2 Double Line To Ground Fault (DLG)

A DLG fault is implemented on node 842 at phase *a* and phase *c*. The absolute sum of d3 for five feeders is shown in Fig. 8. It is noted that the S_{Ia} and S_{Ic} are higher than S_{Ib} in all feeders. As expected, the magnitudes of the absolute sum of the two faulted phases high frequency currents are higher than the threshold value. Fig. 9 illustrates the classification logic output. It is shown that, phase a and c in all feeders have a logic output of "1" at arc fault instant.

In order to find out the faulty feeder the general technique has been applied for five feeders. The output of this technique for DLG fault at phase a, and c is shown in Fig.10. it can be seen that feeder 3 have a logic output of "1" at arc fault instant. Therefore, the detected fault is DLG at two phases a, and c of feeder 3.

3.3 Three Phase Fault (3LG)

A 3LG fault is implemented on node 842. The performance of detector S_I for different phases and feeders is shown in Fig. 11. As expected, the magnitudes of all phases high frequency currents are much higher than the threshold value. The output of the faulty feeder detection approach is shown in Fig.12. It is clearly that feeder 3 has a logic output of "1". So, the faulty feeder is feeder 3. Fig.13 illustrates the classification logic output. It is shown that, three phase in all feeders have a logic output of "1" at arc fault instant.

Therefore, it is clearly seen that, the proposed approach successes to detect the HIF location and to classify the fault type in all cases; single line to ground fault, double line to ground fault, and three phase fault. The scenario of applications proves the simplicity and accuracy of the proposed approach. The proposed approach is independent on the load type or the load balance.

4. Conclusions

This paper introduces an accurate approach for detecting and classifying the HIF in distribution systems. The presented approach recognizes the distortion of the current waveform caused by the HIF arc using DWT. The intelligence of the presented approach is based on three simple logic functions. The logic functions are designed to classify not only the fault location, but also the fault type.

The IEEE 34 node benchmark distribution system is used for the presented approach validation. Different scenarios using Matlab-code simulation are applying three fault types; SLG, DLG, and 3LG.

It is clearly seen that, the presented approach accurately successes to detect and classify the fault location and the fault type in a simple way. Furthermore, the presented approach is independent on the load type or the load balance. This technique is simple, accurate, and fast. It could be used for updating, improving of the existing protection systems, since this algorithm can be added to the existing digital relay microprocessor.

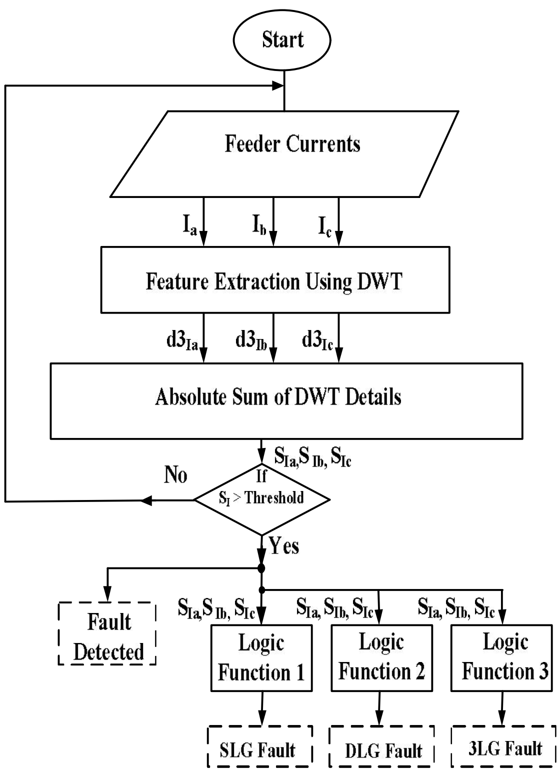
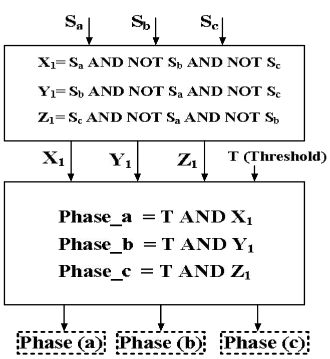
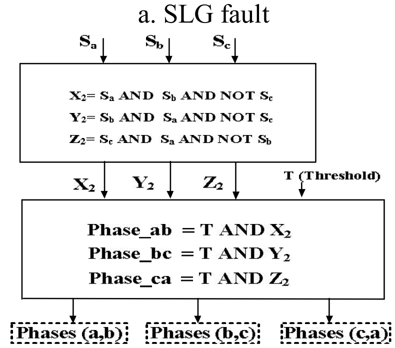


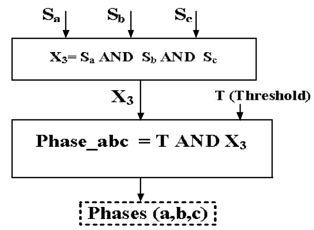
Fig. 1: The proposed detection approach



a. SLG fault



b. DLG fault



c. 3LG fault

Fig.2: The proposed logic functions used for classifying the fault type

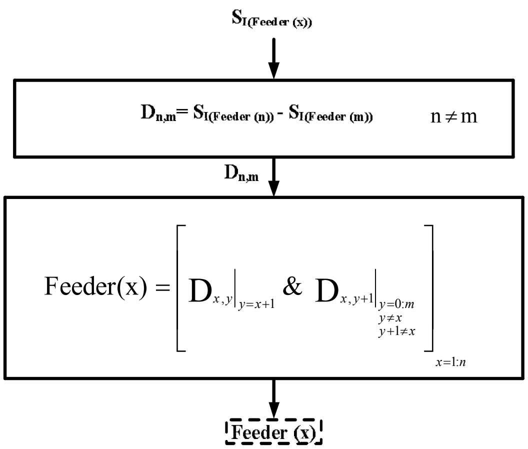


Fig.3: The proposed general approach used for faulty feeder detection

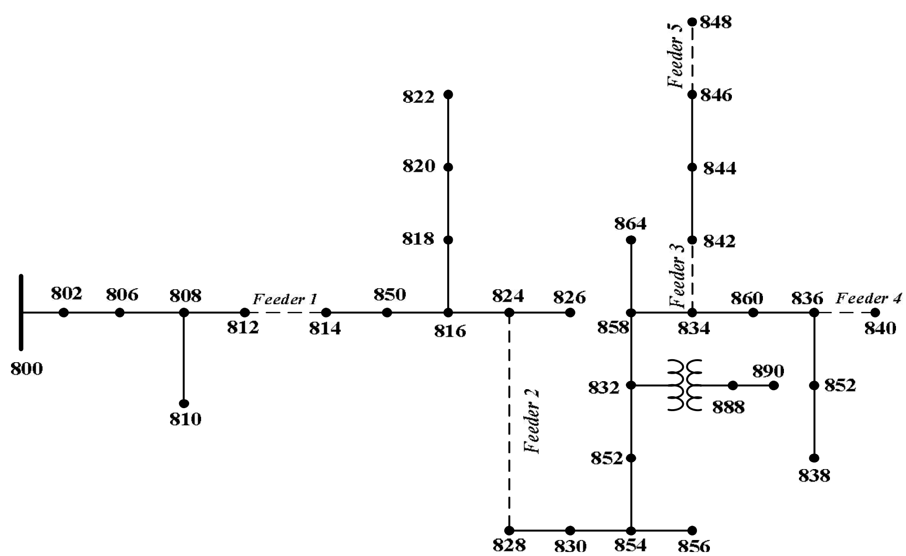
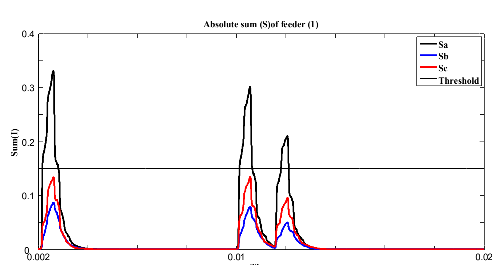
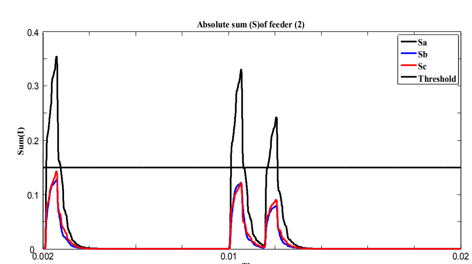


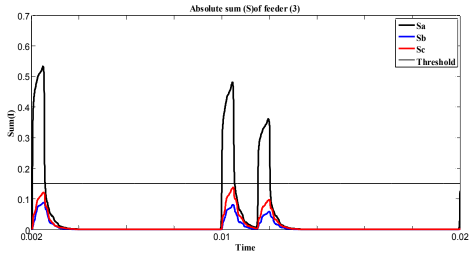
Fig.4: The IEEE-34 node test feeder system



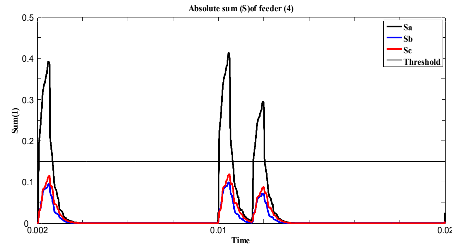
a. Feeder 1



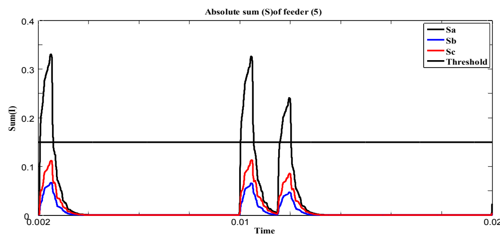
b. Feeder 2



c. Feeder 3

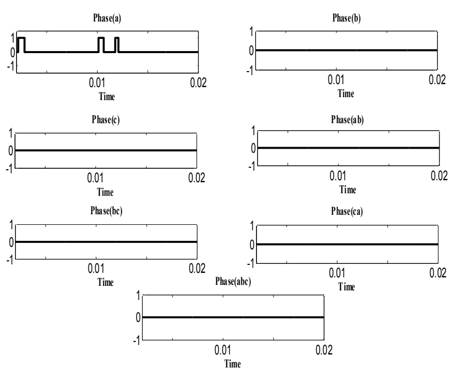


d. Feeder 4

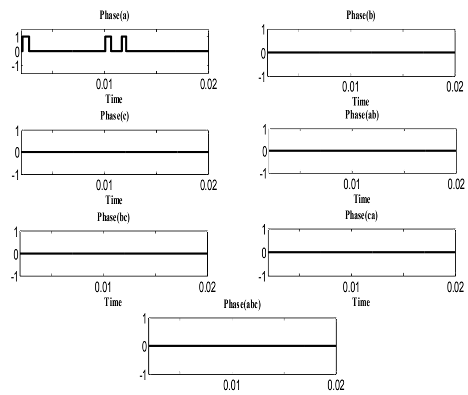


e. Feeder 5

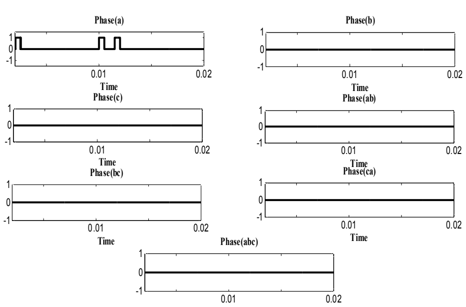
Fig. 5: The absolute sum of d3 for all feeders at SLG fault



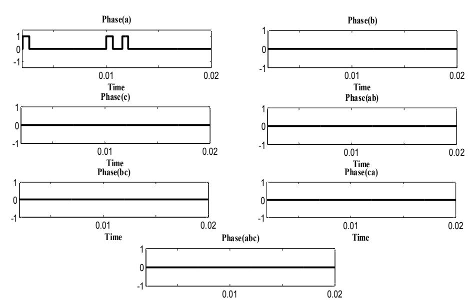
a. Feeder 1



b. Feeder 2



c. Feeder 3



d. Feeder 4

Fig.6: Output of logic function 1 for SLG

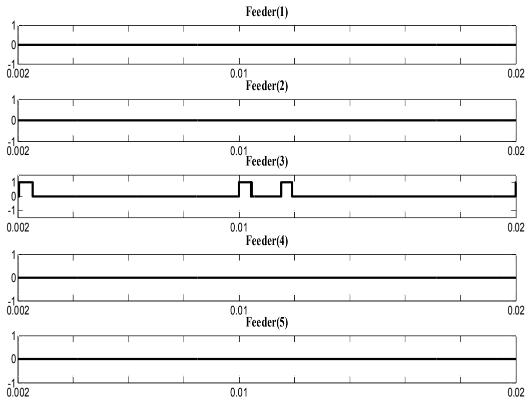
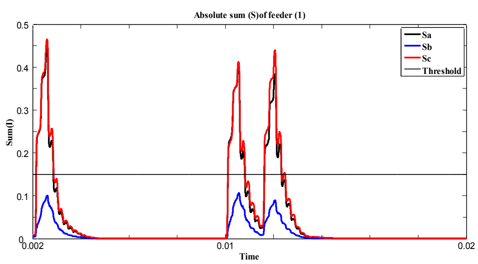
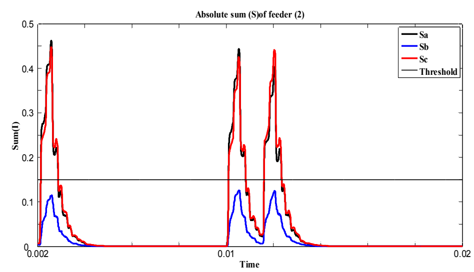


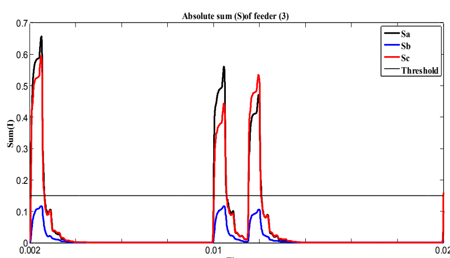
Fig.7: Output of faulty feeder logic function at phase *a* in all feeders for SLG



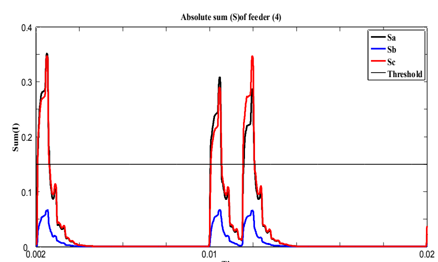
a. Feeder 1



b. Feeder 2

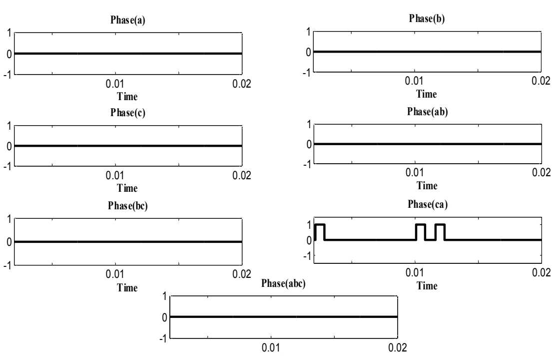


c. Feeder 3

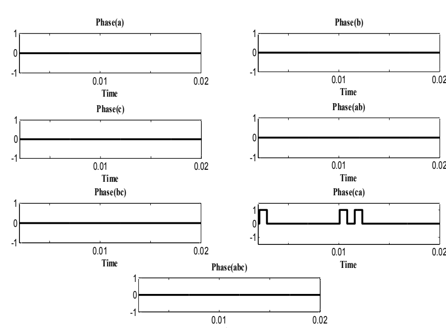


d. Feeder 4

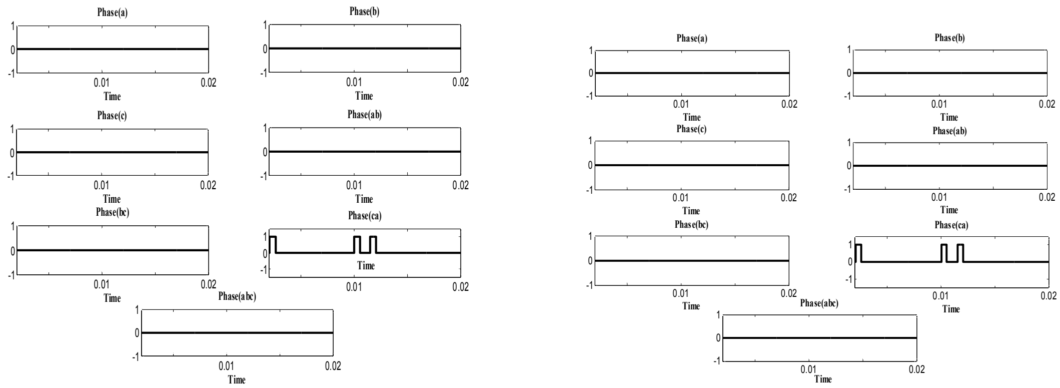
Fig. 8: The absolute sum of d3 for all feeders at DLG



a. Feeder 1

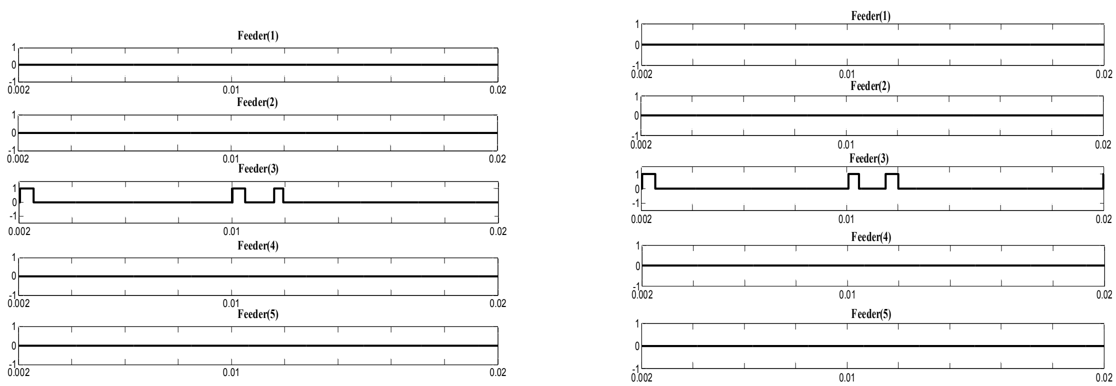


b. Feeder 2



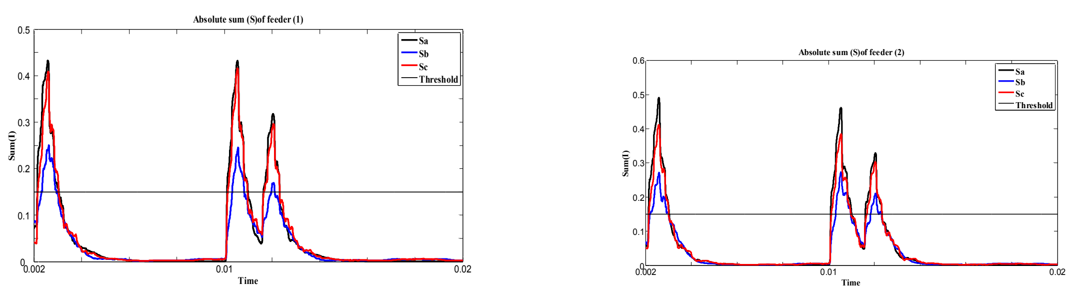
c. Feeder 3 d. Feeder 4

Fig. 9: Output of logic function 2 for DLG

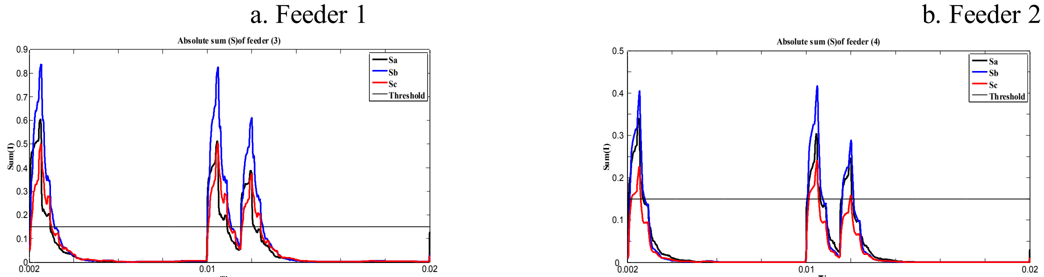


a. phase a b. phase c

Fig.10: Output of faulty feeder logic function at phases *a*, and *c* in all feeders for DLG

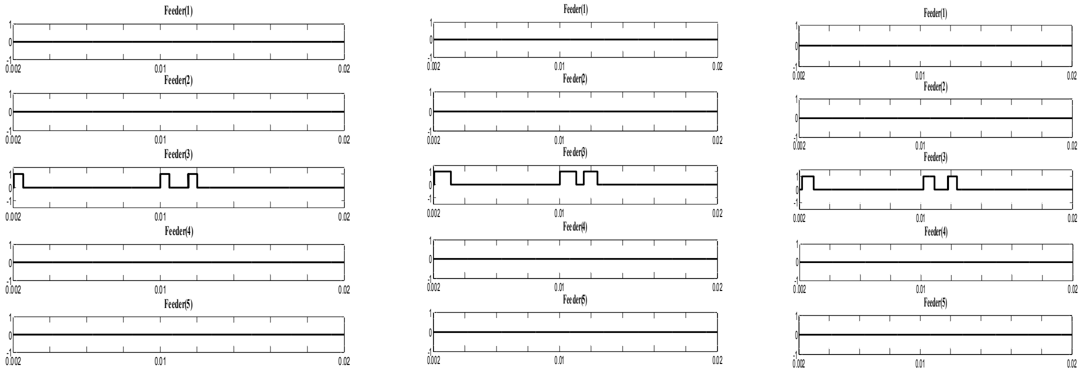


a. Feeder 1 b. Feeder 2



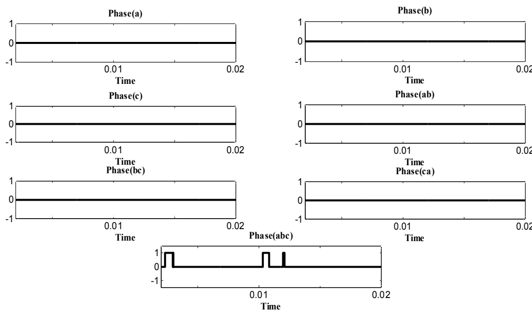
c. Feeder 3 d. Feeder 4

Fig. 11: The absolute Sum of d3 for all feeders at 3LG

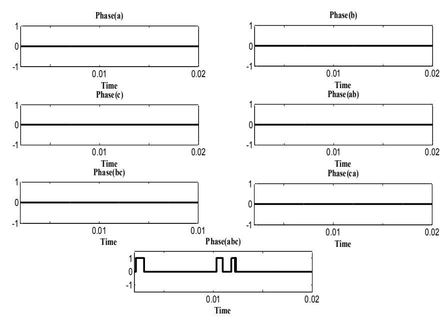


a. phase a b. phase b c. phase c

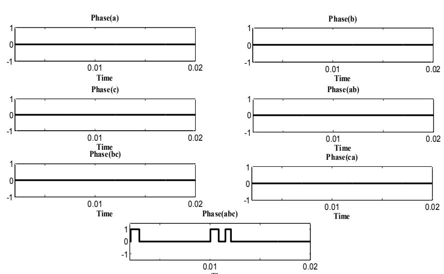
Fig.12: Output of faulty feeder detection in all feeders for 3LG



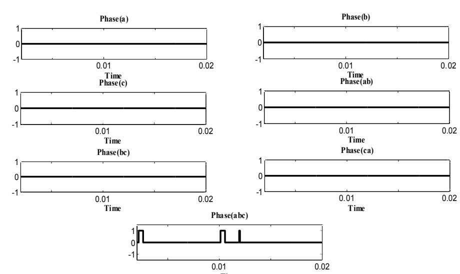
a. Feeder 1



b. Feeder 2



c. Feeder 3



d. Feeder 4

Fig.13: Output of logic function 3 for 3LG

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