Design Of Optimal Xor Gate Based On Quantum Cellular

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Abstract: Today Quantum Cellular Automata (QCA) has been presented as a pioneer technology in design of computers of new generation. QCA facilitates computerized calculations on nano level; and in the light of its simple concepts and capabilities it is highly given attentions to. Considering the significance of such parameters as length of transfer paths of bit stream, the occupied area and modality of clock determination, substitution of primary structures of logic circuits in QCA is of high significance. In this essay a new method for implementing an XOR gate has been suggested. The suggested method benefits from the inherent characteristics of QCA in timing and directing data flow and clock phases; therefore, this suggested structure shall have lesser cells in comparison with the existing implementation methods. The suggested simulation has been performed with the help of QCA Designer tools and has been compared with the existing methods in terms of number of cells and surface area.
[Mostafa Sadeghi, Masoud Shafiee, Faezeh Memarzadeh-Zavareh. **Design Of Optimal Xor Gate Based On Quantum Cellular.** *J Am Sci* 2012;8(12):1032-1036]. (ISSN: 1545-1003). http://www.jofamericanscience.org. 140

Keywords: Quantum Cellular Automata (QCA), XOR

1. Introduction

Forty years ago, Gordon Moor presented his famous theory on global development of electronic industry. According to this theory, which is converted to a Law, in each 18-month period the number of elements mountable on a specified surface area will be doubled. Figure 1 shows the graph of Moor's law. But evidences show that the so-called CMOS technology will finally reach to its physical limitations and will have no possibility for being smaller. In order to preserve Moor's law, some researches are being conducted all over the world for substituting new technology.

Quantum-Dot Cellular Automata or in brief QCA is among these technologies that have capability for reaching to a higher densities of elements (about 1012 elements/cm2), a very high speed (within the range of terahertz), and very low rate of loss of power (Askari et al., 2011). Computation by QCA cells will be done in relation to the neighbor cells and the impact of each cell on polarity of the neighboring cells. Each QCA cell includes four quantum points. Each quantum point may be a small piece of a semi-conductive or metallic part with a minute diameter. Each cell contains two moving electron that may be displaced between quantum points (Dehkordi et al., 2011). Figure 2 shows a QCA cell. By coulomb repulsion force, two electrons will be forced to be placed at the extremes of a diameter. Therefore, two separate and sustainable polarities like as figure 3 will be created, one representing positive polarity or bit 1, and the other representing negative polarity or bit 0.

Whereas QCA has many capabilities and some of them are not exist in CMOS technology, design of circuits based on QCA technology has been paid attention to. In (Wang et al., 2003 and Zhang et al., 2005) the primary quantum structures for one-bit adder have been presented and then an optimal method with lesser gates and cells has been presented in (Xiaojun et al., 2008). In (Mathew et al., 2008) a multi-bit adder has been presented which has transferable digit prediction capability. Among other works carried out in the field of QCA circuits we may point out design of RAM (Vankamamidi et al., 2008 and Shamsabadi et al., 2005), and deign of primary FPGA (Ottavi et al., 2005) and serial adder (Taskin et al., 2008). Adder is the main and basic part of a microprocessor; and implementation of this part shall be numerated as a significant part in each technology. In the light of electrostatic aspect of this technology placing circuits and overpass of two different wires shall be very important in design procedure. Simulations show that crossing point of two wires is one of sensitive points in QCA circuits. This means that any defect around these points at the time of production may cause failure in performance of circuit.

In continue of this essay these sections will be presented: in section 2, the basic logics in QCA will be introduced and we will state timing and modality of works of clock in QCA. In section 3, deficiency and failure models of this technology will be analyzed in brief. In section 4, we will pay a review on XOR gate and an analysis of the new method, in section 5 we will represent simulation and

test of the suggested method, and in section 6 we will present conclusion and results.

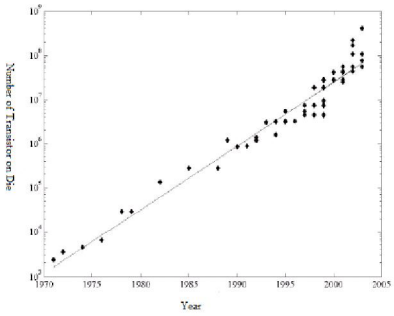

Figure1.

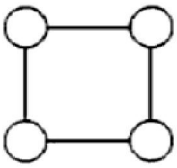

Figure 2. QCA cell

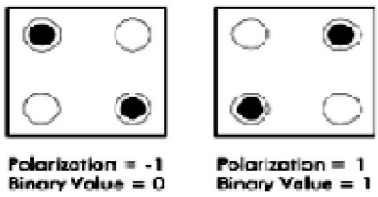

Figure 3. Polarization status of cells

2- Basic Logics and Failure Models

2-1- QCA-Based Wires

With the help of serializing quantum cells it would be possible to transfer binary quantities from a cell to another one along a specific length. Dispersion of bits along paths is the result of repulsion of electrons of adjacent cells, the modality of which has been shown in figure 4. As it is visible in figure 4, cell 1 is coerced to change its polarity to +1. Therefore, cell 2 will be converted to +1 as the result of repulsion between electrons; and other adjacent cells shall also pass such trend so that finally new polarity will be reached to cell 9. Whereas polarity is imposed to cell 1 from the outside, change in polarity will not be occurred reversely.

Figure 4. Wire's Model in QCA (90 degree)

With serializing cells, we can produce copper wires with 45° angle of rotation. In this way, as figure 5, polarity of adjacent cells shall be opposite to each other. The privileges of this type of path is attaining to positive and negative poles without need to inverter.

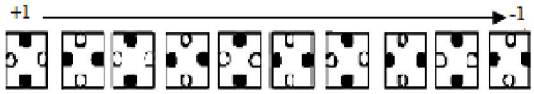

Figure 5. Wire's Model in QCA (45 degree)

2-2- Inverter Gate

As described before, a method for inverting bits is the use of 45-degree rotated cells along the wire. If we want to use ordinary cells we should put cells aside of each other in accordance with figure 6-A. in the light of repulsion that parallel cells may impose on the corners of output cells, their polarities will become opposite to parallel cells. Also figure 6-B shows another structure of inverter which works by tunneling property.

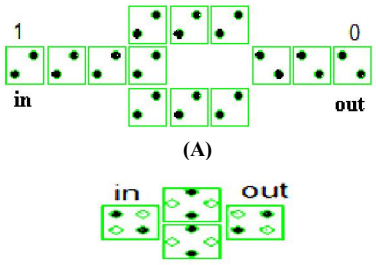

Figure 6. (A) Inverting Gate of QCA. (B) Inverting Gate of QCA

2-3- Majority Gate

Majority gate is the main unit in design of QCA-based logic circuits; the structure of which has been shown in figure 7. This structure has been formed by three input cells, a central cell called as device cell and an output cell.

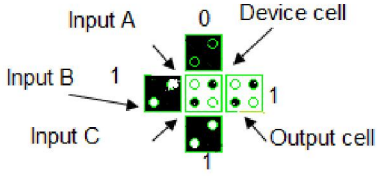

Figure 7. Majority Gate of QCA

In the light of repulsion between electrons, polarity of central cell shall be subject to the status of majority of input cells i.e. the more number of input cells with the same polarity will impose much force on the same direction and will overcome the force imposed by cells with opposite polarity; therefore,

device cell and consequently output cell will reach to dominant polarity. In figure 7, existence of two cells with +1 polarity will lead to a change in polarity of device cell and output cells to +1; and we could show it as equation 1.

$$M(A,B,C)=AB+AC+BC \quad (1)$$

If in the majority bits polarity of one input cell stands at -1, two other inputs should be +1 so that their force may overcome -1; and the output will become +1. This output is the result of AND operation; and we may use this method for implementing AND gate

$$M(A,B,0)=AB+(B0)+(A0) \quad (2)$$

If in majority gate the quantity of one input is put on +1, it is clear that if at least the quantity of one another input cell is put on +1, the output will definitely be +1 i.e. this structure shows the behavior of OR gate; therefore, we may implement OR gate by this method:

$$M(A,B,1)=AB+(B1)+(A1)= AB+B+A=A+B \quad (3)$$

2-4- Clock in QCA

QCA as all other electronic technology shall need clock pulse. But clock at this technology shall be a source of power supply for running these circuits further to synchronizing and control of data flow. Despite CMOS technology, clock pulse in this technology works at four phases. In the first phase of clock, known as switch phase, cells of one sub-arrangement will lose their polarities; and then will take polarity in relation to polarities of input cells; in fact, computation will be performed in this phase. At the end of this phase, inter-cellular carriers shall have maximum potential; and no change may be occurred in polarities of cells. In fact in the next phase, called hold phase, the status of sub-arrangement cells will remain fixed, and the output of one sub-arrangement may be the input of another one. In the third phase, known as Release Phase, potentials will be reduced and cells will be permitted to lose their polarities. In the fourth phase, i.e. the Relax Phase, cells in sub-arrangement will also remain in the status of unpolarized. Figure 8 shows the said four phases.

3- Failure and Defects Models

At this part, different models of defects in QCA technology will be studied in brief. These defects shall mainly be divided in two parts: cellular displacement defects and cellular shortage defects.

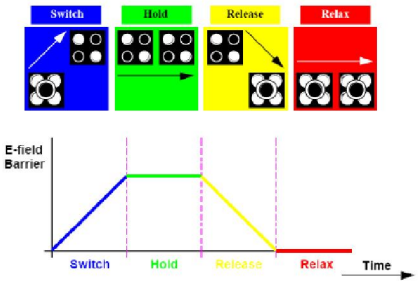

Figure 8. Four clock phases in QCA

3-1- Cellular Misplacement

Cellular misplacement is a defect in which a cell is not placed in its exact place; in another word it may be displaced a little (Huang et al., 2007). Figure (9-A), is a status without defect; and figures (9-B) and (9-C), show two cases of such defects in MV.

2-3- Cell Shortage

Cell shortage is a defect in which a cell is not put in its right place at the time of placement in a circuit. In fact, the defected circuit has a cell less than the state of complete form. Figure (9-D) shows a case of such defect in one of MV's inputs:

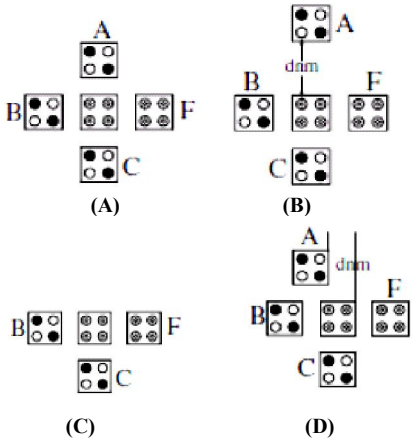

Figure 9. (A) Without Defect, (B) Misplacement of Cell A (C) Misplacement of Cell A, (D) Shortage of Cell

4- XOR Gate

In this part, we will pay attention to the procedure of design of XOR gate as a basic part of design of logic circuits and will study its existing structure; and then will introduce the suggested optimized structure.

4-1- XOR Gate

One of frequently-applied gates for implementing different types of circuits for adding, deducting, multiplying etc. is XOR gate. The

exclusive OR (XOR) shown by the mark of ⊕ is a logical operator that implements the following Boolean function:

$$X \oplus Y = XY' + X'Y \quad (4)$$

This function will only be equal to 1 when x or y is equal to 1, but not concurrently being 1; and in accordance with figure 10 it shall be designed on logic level with two gates of NOT, two gates of AND, and one gate of OR. Implementation of this gate in QCA is visible in figure 11. As it is seen in this figure, for implementation we need two inverting device and three gates of majority. The results of simulation have been shown in figure 12, the transfer of input to output of which shall be performed in 4 clock phases.

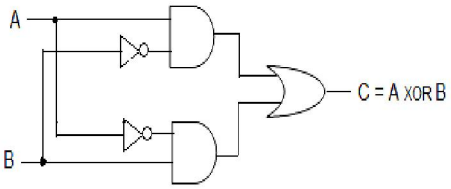

Figure 10. Design of a gate of XOR

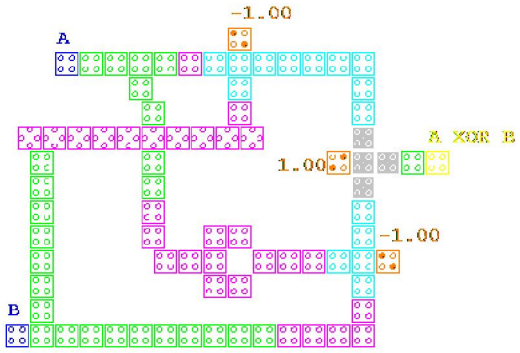

Figure 11. Implementation of a two-input gate of XOR in QCA

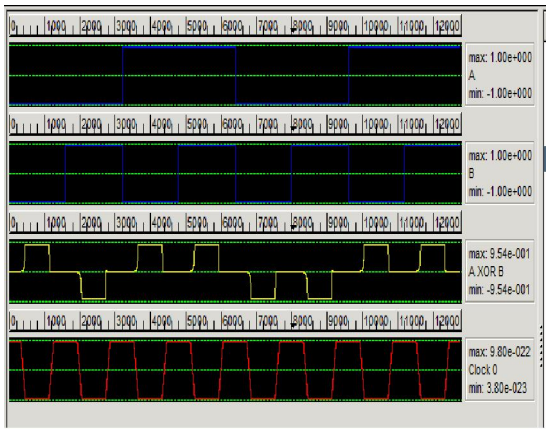

Figure 12. Results of Simulation of an XOR Gate

4-2- The Suggested Optimized Method

In the method seen in the previous part, about 80 cells shall be needed for implementing the gate of XOR; and 4 clock phases will be used for production of output. Whereas the surface area and lengths of wires are the barriers to implementation of this gate, in this paper a method with lesser number of cells and the required area and with a higher speed, is suggested for implementing XOR gate.

5- Simulation and Test of the Suggested Method

The suggested XOR gate is simulated in QCA designer (figure 13), and the results have been shown in figure 14:

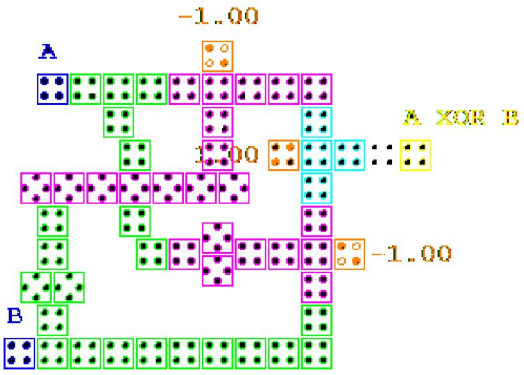

Figure 13. Design of the Suggested XOR

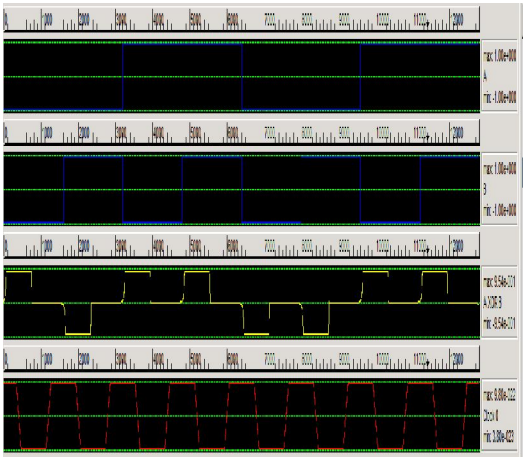

Figure 14. Results of Simulation of the Suggested XOR gate

As it is seen in figure 14, when Clock 3 is in the verge of descending edge, the output rate will become equal to XOR gate. In this design we used about 55 cells, optimized 31.50 % in comparison with the previous design (using 80 cells); while the occupied area is about 60% of the area of previous design. Meanwhile, in this design, transfer of input to output shall be performed in 3 clock phases, representing 25% more speed than the previous

design (in which transfer is performed in 4 clock phases).

6- Conclusion

As it was pointed out, design of QCA-based circuits has been given attention for their characteristics. Therefore, designing basic structure with lesser cells and shorter paths would be effective in optimization of output quality, and in reducing complications and dimensions of circuit. In this paper, a new structure has been suggested for XOR gate that uses a lesser number of cells in comparison with the previous method, while the speed of transfer of input to output is more than this speed in the previous design.

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8/12/2012